The BC-1 Power Amplifier

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The BC-1 amplifier design was covered in the second edition of *Designing Audio Power Amplifiers* [1]. Here we describe what it takes to build a complete and working amplifier by describing the BC-1 power amplifier in detail. Build and test issues are also discussed. This amplifier is not sophisticated, but yields very respectable performance and it is designed to be robust.

The amplifier employs two output pairs and produces about 125 watts into an 8-Ω load with ±52 V rails (under load). It is possible to design for lower or higher power by changing only the rail voltages and adding additional output pairs and heat sinking for rated power levels above 150 watts. Key performance characteristics include:

- 125 W into an 8-Ω load with ±52 V power rails
- Full-power THD+N of 0.0006% at 1kHz, 0.007% at 20 kHz
- Un-weighted SNR of 105dB in an 80-kHz noise bandwidth
- 7.5 nV/√Hz input-referred noise density
- High-current output
- Stable with high performance into a 2-Ω load
- Scalable to higher-power implementations

1. The Basic Design

The schematic of the front end is shown in Figure 1. Features include:

- Gain set to 29 dB so that 1 Vrms generates 100 W into 8 Ω
- Locanthi triple emitter follower output stage
- Quasi-differential input/feedback network
- Diode clamps across the feedback network capacitor for fault protection
- Diode clamps across input differential pair for transistor protection
- Diode clamps across the IPS differential outputs for cleaner clipping
- Unity loop gain frequency (ULGF) of 1 MHz
- VAS output Zobel network for increased stability
- Dual V_{be} multiplier bias spreader with bypass/reservoir capacitor
- Current limiting diodes from the bias spreader to the output rail
- Fast output transistors (MJL3281/1302)
- Rail reversal protection diodes
- Progressive rail decoupling
- Comprehensive amplifier and loudspeaker protection circuits
- Power on/off muting

2. The Front–end: IPS, VAS and Pre-drivers

The front-end of the amplifier, comprising the input stage (IPS), voltage amplifier stage (VAS) and output stage (OPS) is shown in Figure 1. It includes all of the amplifier circuitry up to and including the pre-drivers. It is implemented on its own board. The output stage, including drivers, is implemented on a second board that is mounted on the heat sink. The protection circuits are implemented on a third board.

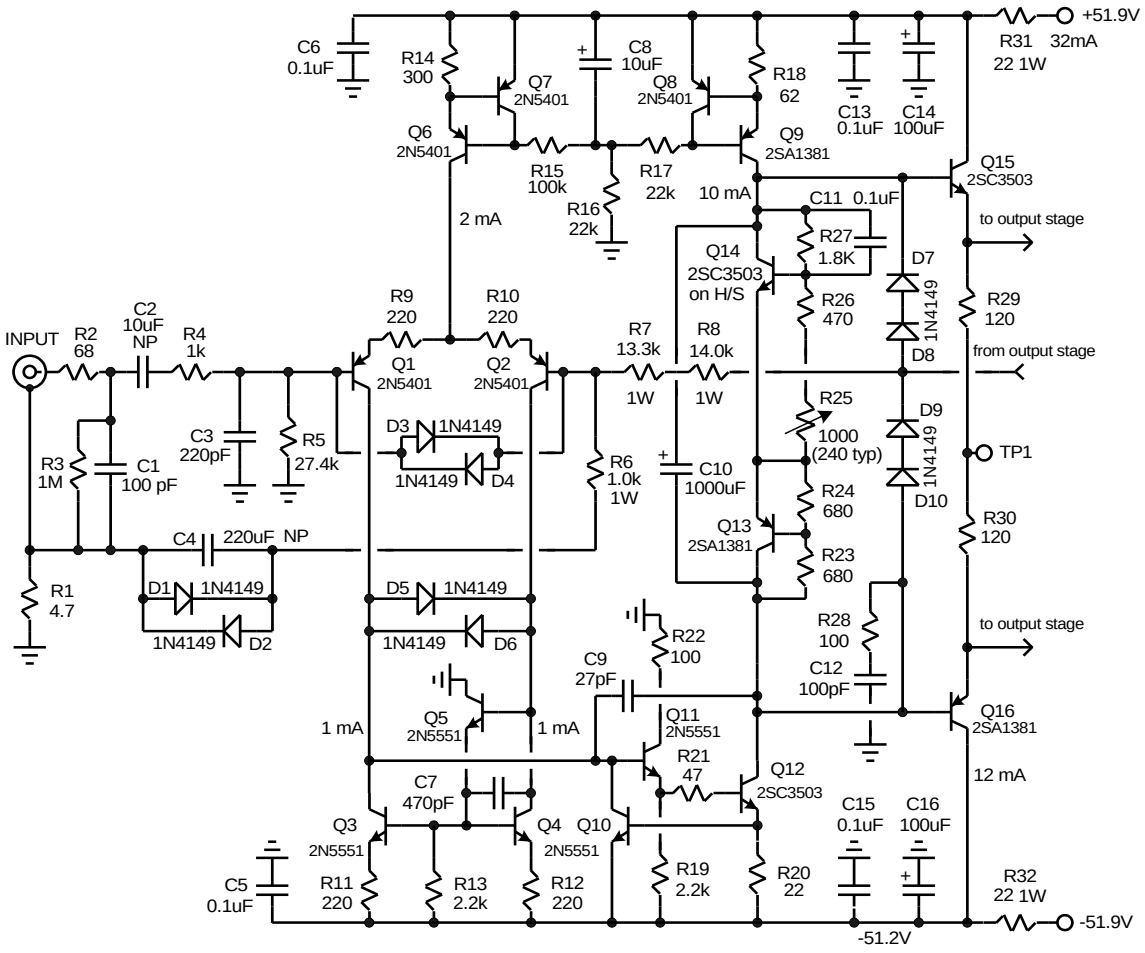

Figure 1: Amplifier front end

Input Network

The main part of the power amplifier can be viewed as a power operational amplifier. Looking closely at the input and feedback networks, one can see that the amplifier is configured somewhat like a single op-amp differential amplifier. This provides some common mode rejection to signals that exist at both the shield and center conductor of the input cable.

The first input low-pass filter formed by R2 and C1 has two purposes. First, it provides a roll-off at 23 MHz. This is the first line of defense against high-frequency EMI

at the input. Secondly, it terminates the input interconnect at approximately its characteristic impedance at high frequencies (68 Ω is a compromise between the typical values of 50 Ω and 75 Ω of shielded interconnect). The second, and more conventional, input low-pass filter is formed by R4 and C3 with a corner frequency at 720 kHz. The 10-μF NP electrolytic coupling capacitor and 27-kΩ shunt return resistor create a roll-off at 0.6 Hz.

Resistor R1 (4.7 Ω) isolates the RCA connector ground from the circuit ground. This reduces the effects of ground loops. The 1-kΩ negative feedback shunt resistor R6 is returned to the RCA connector ground through C4, a 220-μF NP electrolytic capacitor. This arrangement, in combination with the small attenuation of R4 against R5, gives the amplifier some of the properties of a differential input. The feedback resistor is comprised of two 1-W metal film resistors in series (R7 and R8). This minimizes resistor voltage and temperature distortions in this critical location. Shunt resistor R6 is also a 1-W metal film type. Together, these resistances establish the closed-loop gain to be 27.3, not including the 0.5 dB loss created by R4 and R5. The reasonably low impedance of the feedback network provides a good compromise between low noise and the amplifier input resistance of 28 kΩ.

The feedback resistance consists of one 13.3-kΩ resistor in series with one 14.0-kΩ resistor, both available in E48 or E96 series values. An approximate center tap is made available by the use of 2 feedback resistors in series. It can be used for phase margin and gain margin testing to be described later. A smaller feedback network impedance can be used to reduce noise a bit, but this will require a smaller input return resistor unless DC offset is to be incurred.

The IPS input return resistor R5 is made equal to the feedback resistor value. This balances out the effect of input transistor base currents if they are equal. At 1 mA collector current, base current of the IPS is 10 μA for transistor beta of 100. This 10 μA flowing through 27.4 kΩ creates a 274 mV drop. If beta of the two input transistors is matched to 10%, the offset voltage will be only 27 mV at the amplifier output. This underscores the need for reasonable beta matching of the input pair.

Feedback Network

The non-polarized electrolytic decoupling capacitor C4 brings the gain down to unity at DC. This minimizes DC offset at the output. The 220-μF, 100-V NP capacitor creates a 0.7-Hz low-frequency corner against R6. It contributes virtually no electrolytic capacitor distortion because of its high voltage rating [1]. This capacitor is made by Nichicon for use in loudspeaker crossovers (UKZ2A221MHM). Nevertheless, it is often recommended that such electrolytic capacitors in critical locations be bypassed with a film capacitor. Although not shown on the schematic, 1-μF polypropylene capacitors have been placed across both C2 and C4. Bypassing C4 also minimizes any effects of inductance in C4 on the feedback network at high frequencies. Clamping diodes D1 and D2 across C4 prevent high voltages from appearing in the event of a fault where the output is stuck at a rail. Although C4 can withstand 100 V, such a voltage could damage the input stage.

Input Stage (IPS)

The design includes a degenerated long-tailed pair (LTP) input stage (Q1 and Q2) with a current mirror load and a Darlington VAS, as shown in Figure 1. The tail current is 2 mA and the degeneration resistor values are 220 Ω. Base-to-base protection clamp diodes D3 and D4 prevent the input differential pair transistors from ever seeing a large base-emitter reverse bias that could cause Zener breakdown of the base-emitter junctions under fault conditions. Base-emitter breakdown is only 6 V for the 2N5551. Breakdown conduction can damage the input transistors and cause beta degradation. The diodes chosen are 1N4149, which are similar to the venerable 1N4148, but with lower capacitance. The IPS and VAS current sources share a common intermediate filtered voltage (25 V) across C8 from which they are energized.

The current mirror comprised of Q3 and Q4 includes an emitter follower "helper" transistor Q5 that supplies the base current for the mirror transistors. This improves mirror accuracy and causes the collectors of both IPS transistors to be at the same DC potential as a result of the 2-V_{be} input voltage of the 2-transistor Darlington VAS. Emitter degeneration voltage drops in the current mirror and VAS are made the same. The equal IPS collector voltages enable the use of anti-parallel 1N4149 clamp diodes D5 and D6 across the IPS collectors to limit and equalize the voltage swings under clipping conditions. This mitigates some clipping artifacts and limits over-current in the VAS Darlington transistor Q11 under negative clipping conditions. A 470-pF compensation capacitor C7 has been placed from base to emitter of the helper transistor to reduce its role at very high frequencies, improving local stability without compromising the bandwidth of the current mirror. It also reduces HF interactions between the current mirror and VAS Miller compensation at high frequencies.

Voltage Amplifier Stage (VAS)

The two-transistor VAS enjoys good performance due to the speed and minimal Early effect of the 2SC3503 main transistor Q12. The VAS current limiting transistor Q10 is a 2N5551 with V_{be} = 0.66 V @ 2 mA. In combination with R21 = 47 Ω, this creates a 30-mA current limit.

The emitter follower Q11 of the 2-transistor VAS can sometimes be subjected to excessive current when negative clipping occurs. In a normal arrangement, when negative clipping occurs, the IPS output will try to turn on the VAS transistor harder. This is especially the case when a current mirror load is used. Nearly all of the IPS tail current will try to flow into the base of the first transistor of the 2T VAS. That transistor will source significant current from its emitter into the base of the saturated VAS transistor, ultimately flowing into its emitter and emitter degeneration resistor. Collector current spikes of at least 20 mA can occur in the first VAS transistor. Since this transistor has nearly the full rail voltage across it, there may be safe area concerns. A limiting resistor R21 that operates in conjunction with the IPS output clamps is placed in series with the base of the VAS transistor.

The limited voltage swing from the IPS as a result of the collector clamp diodes limits the amount of current that can flow in Q11 because of the drop across the VAS emitter resistor. When negative clipping occurs, the input to Q11 increases by only one diode drop. However, this alone does not sufficiently limit collector current in Q11. To further limit the current, a 47-Ω resistor is placed in series between the emitter of Q11 and the base of Q12. Excess current flowing from Q11 into the base of now-saturated Q12 will create a voltage drop across this resistor that will create a self-limiting effect on the current in Q11. Current will be limited to a much safer 6 mA. With 52-V rails, Q11's dissipation will briefly be about 300 mW.

Compensation capacitor C9's value of 27 pF, sets the gain crossover frequency (ULGF) to just below 1 MHz. C9 should be a ceramic COG capacitor rated at 100 V or more for best linearity. A small Zobel network comprising C12 and R28 has been added in shunt with the VAS output node to improve stability at frequencies above the ULGF. It ensures that the impedance at this node remains positive resistive at very high frequencies. This is especially helpful when output stage Triples are employed. The Zobel has little effect on the global compensation scheme and detracts minimally from slew rate. Note that on positive clipping the Miller shunt feedback around the VAS becomes inactive and the VAS output impedance may go high, potentially causing instability in the output stage. The VAS output node Zobel network prevents this.

The pre-driver emitter resistor is actually made up of two equal resistors (R29, R30) in series. This provides a center tap for testing purposes. It allows the feedback loop to be closed from the pre-driver output. This is especially handy for testing the front-end board by itself. It also allows measurement of output-stage open-loop distortion.

Bias Spreader

In contrast to the simple V_{be} multiplier bias spreader used in many amplifiers, a 2-transistor dual V_{be} multiplier comprising Q13 and Q14 is used. If all of the pre-driver, driver and output transistors are mounted together on the main heat sink, then a single-transistor bias spreader with its transistor also mounted on the heat sink provides reasonable temperature compensation, since all of the transistors will be at about the same case temperature.

Here a different approach to mounting the pre-driver and driver transistors has been chosen. The pre-driver transistors are not mounted on the main heat sink. They are thus at a different temperature from the driver and output transistors. The pre-driver transistors are best compensated with a separate V_{be} multiplier. One of the V_{be} multiplier transistors, Q14, is mounted on the heat sink and the other is mounted on the circuit board.

The dual bias spreader design employs a complementary pair of V_{be} multiplier transistors connected in series. One transistor, Q14, is used to temperature compensate the driver and output transistors while the other, Q13, compensates the pre-driver transistors. A bias trim pot is included in the Q14 V_{be} multiplier. A TO-126 NPN V_{be} multiplier transistor (2SC3503) is mounted on top of one of the power transistors with the

same screw that holds the power transistor to the heat sink. Thermal grease is used at the interface. The insulated TO-126 case of the 2SC3503 can be easily mounted to the heat sink or onto the case of one of the output power transistors. It serves to temperature-compensate the output transistors and the drivers with a spreader voltage of ~ 4 V_{be}. A TO-126 PNP V_{be} multiplier transistor (2SA1381) is sandwiched between the pre-driver transistors on the front-end board, with heat sink compound at the interfaces of the three transistors. A single screw with washers on either side holds the three TO-126 transistors together. Its spreader voltage is ~ 2 V_{be} to furnish the bias required by the pre-drivers. Total dissipation of the two pre-drivers is about 1.3 W. A small on-board heat sink is mounted to the group of 3 transistors. Alternatively, Q13, Q15 and Q16 can be mounted on a common heat spreader that also acts as a modest heat sink.

The dual bias spreader arrangement provides good stability during warm-up and does not subject the pre-drivers to the potentially significant thermal variations of the main heat sink that are a function of power output. The pre-driver transistors operate at nearly constant power in class A, so there is no reason to subject them to such thermal variations. The dual-V_{be} twin bias spreader approach is especially helpful to bias stability in Triple EF output stages because of the number of V_{be} drops (6) that are stacked up in the Triple EF.

An unusually large 1000-µF bypass capacitor has been added to the bias spreader. The large-value capacitor acts like a reservoir capacitor for the bias spreader in the event that current through the VAS goes to zero during positive clipping. This minimizes the impact of bias spreader collapse under these conditions. Such a collapse can create a time-dependent discharge of bias voltage, resulting in biasing error hangover effects that may persist after the clipping interval. This occurs on only one-half clipped cycle with a single-ended VAS, since the VAS current source does not cut off on negative clipping. This can happen on both half cycles with a push-pull VAS.

Bias spreader collapse can be significant on large-amplitude low-frequency signals, whose half cycle could last 25 ms at 20 Hz. Some fraction of that half-cycle may clip the amplifier. Assume a 15-ms clipping interval and a maximum allowable bias spreader sag of 26 mV (to half idle bias) for sizing the capacitor. The main cause of spreader voltage sag is the discharge of the spreader bypass capacitor by the spreader resistors R23-R27. This assumes that under positive clipping conditions no current is flowing in the bias spreader transistors. If 1mA is being passed through the V_{be} multiplier resistors and a 1000-µF spreader bypass capacitor is being employed, the collapse will be limited to 15 mV.

Current limiting

Two series-connected pairs of 1N4149 natural current limiting diodes D7-D10 are connected from the ends of the bias spreader to the output rail. I also refer to these as “flying catch diodes”. These diodes clamp the VAS output voltage relative to the output rail if the voltage drop across the output emitter resistors exceeds a certain value. This prevents the output stage from delivering more than a set value of maximum current. Consider a total spreader voltage of about 3.8 V and a diode turn-on voltage of 0.6 V.

The voltage at one end of the spreader needs to move by about half the spreader voltage plus a diode drop before the limiting diodes conduct and limit further current increase. In this case, that would be about 2.5 V. With 0.22-Ω emitter resistors, each output transistor will be limited to peak current of about 11 A. The intervention of the short-circuit protection circuit limits the duration of this peak to a very brief interval. If this interval is exceeded, the loudspeaker relay will be opened. In reality, the peak current limit will be a bit smaller than 11 A, since this simple analysis did not take into account the increased V_{be} drops in the output stage under these conditions. For this reason, 2 diodes in series are used.

In the case of an output Triple, where the bias spread is about 6 V_{be}, the clamp diode pair is reverse-biased by 3 V_{be} when no output current is flowing. If enough current flows to cause a 3 V_{be} plus 2 diode drop change at either end of the bias spreader, the diodes will become forward biased and prevent any further increase in output current. Five junction drops here is about 3 V. Much of this change will end up across R_E. If impressed across R_E = 0.22 Ω, this corresponds to a current limit of about 13.6 A per output transistor. At these high currents there will be some voltage drop in the base stopper resistors and increased V_{be} of the output transistors. As a result, the actual current limit is smaller, at about 11 A. With 2 output pair, total output current will thus be 22 A. This high current-limiting threshold allows the amplifier to briefly deliver 44 V into a 2-Ω load.

3. Output Stage: Drivers and Outputs

The output stage and output network are shown in Figure 2. The output stage is a Locanthi Triple with two output pair [1, 2, 3]. The emitter resistor values are 0.22 Ω, making the idle current for each pair 118 mA when the Oliver criteria is satisfied (26 mV across R_E) [4]. This reduces crossover distortion and increases the class A region of operation. Peak class A current is 4 times 118 mA = 472 mA, corresponding to about 1 W into 8 Ω.

The use of a triple emitter follower plays an important role in delivering high output current with low distortion. Many amplifiers just employ a double emitter follower (Darlington) output stage, whose total current gain is only 5000 if the driver transistor beta is 100 and the output transistor beta is 50. Total current gain may be even less when driving high current and the output transistors are suffering beta droop. An 8-Ω will present a load of 40 kΩ to the high-impedance output node of the VAS, requiring the VAS to supply 1 mA when the amplifier is delivering 100 Watts. This is 10% of the VAS 10-mA bias current, and will alter the operating point enough to cause distortion. The situation becomes worse when a 4-Ω load is being driven to 200 Watts and 2 mA or more must be delivered to an output stage that is suffering more beta droop. The situation becomes still worse if a 2-Ω load is being driven to high power and the output stage is suffering even more beta droop. This is a concern even though the amplifier is not designed to deliver the theoretical 400 Watts into a 2-Ω load.

A triple emitter follower will provide total current gain of 100 times that if the pre-driver transistor also has beta of 100. This amounts to current gain of 500,000, requiring the VAS to supply only 40 uA to the output stage when 20 A is being sourced to a 2-Ω load. This also means that the VAS will see a light load of 1 MΩ when a 2-Ω load is being driven.

Unlike some output stages, the pre-driver and driver stages in the Locanthi T circuit operate in class A [1, 2, 3]. This further contributes to low distortion in the output stage.

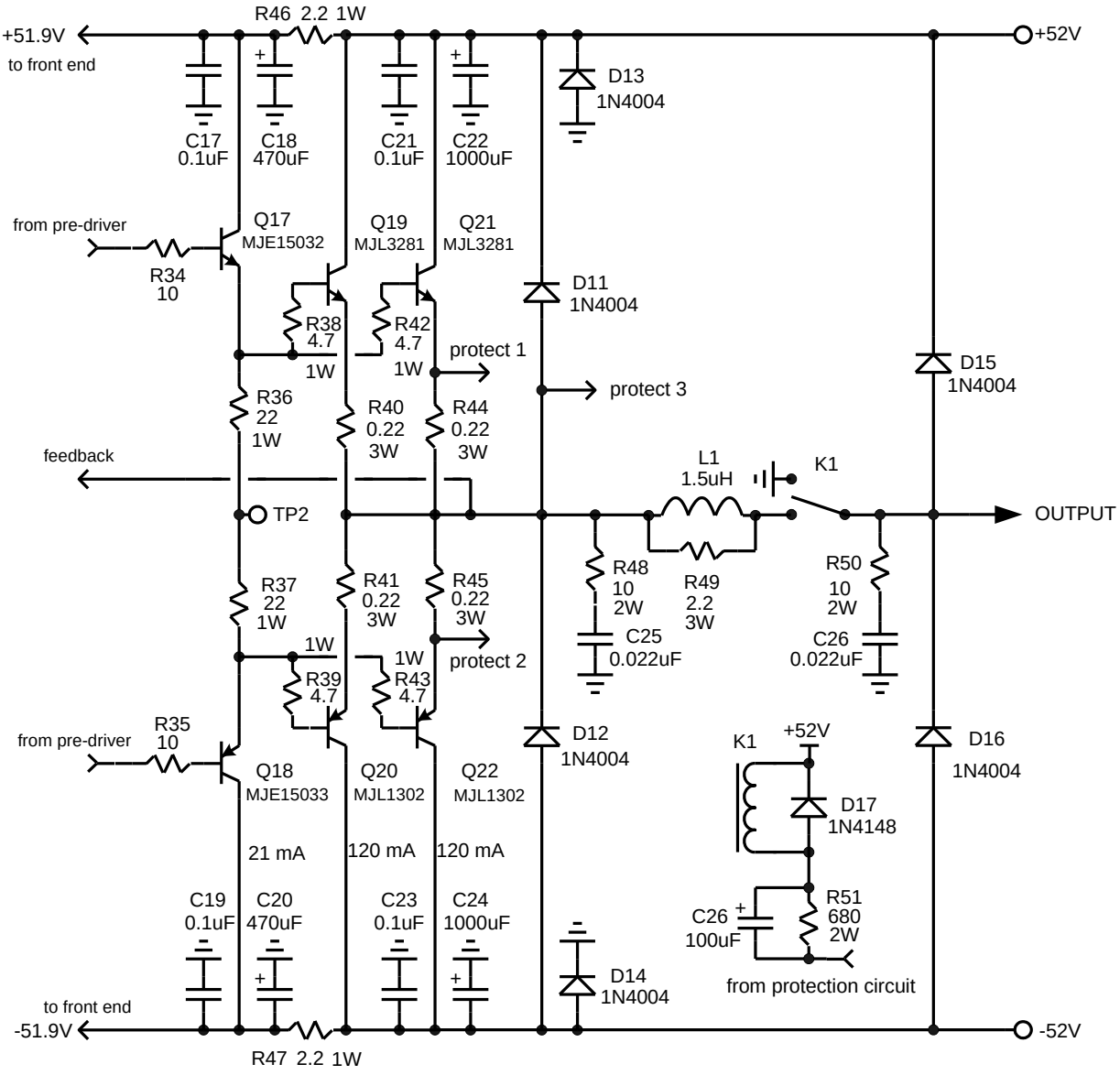

Figure 2: Output stage and output network

The driver emitter resistor is made up of two equal resistors (R36, R37) in series in order to provide a center tap for testing purposes. The healthy 30 mA driver bias current helps turn off the output transistors quickly by depleting stored charge in the base. Base stopper resistors are added in series with each output transistor base to suppress HF oscillations that can sometimes occur when multiple output pairs are connected in parallel. These resistors are 4.7-Ω, 1-W metal oxide film (MOF) types.

The output stage emitter resistors must pass significant current and be capable of dissipating several watts. It is also desirable that they be non-inductive. It has often been common practice to use 5-W non-inductive wire-wound power resistors for R_E. In this amplifier 0.22 Ω, 3-W MOF resistors are used. They have almost no inductance and provide adequate power dissipation capability. The use of wire-wound resistors has been avoided in this amplifier.

Total power dissipation in the R_E resistors can be calculated by recognizing that the net output resistance due to R_E will dissipate a fraction of the power being delivered to the load in proportion to the series resistance they create in the output stage compared to the load resistance. In this amplifier the net output resistance contributed by the R_E resistors is 0.11 Ω under large-signal conditions. This is 2.8% of a 4 Ω load. If the amplifier is delivering 250 W into 4 Ω, the total dissipation in the 4 R_E resistors will be 7 W, and dissipation in each resistor will be less than 2 W.

This amount of dissipation will occur only in continuous full-power testing. For best power dissipation, the emitter resistors should be mounted vertically (one lead coming off the top and down the side) or axially ¼-inch off the board. MOF resistors are capable of passing a large amount of current for brief portions of a cycle without damage or degradation. In the above example, each resistor is called upon to conduct brief peak current of 5.6 A, and drop 1.2 V, for peak dissipation of about 7 W.

The 260-V, 15-A, 200-Watt MJL3281A and MJL1302A power transistors employ a perforated emitter structure to achieve high f_T (30 MHz) and reduced beta and f_T droop at high current. These transistors also have good safe operating area.

Protection diodes D11 and D12 are connected from the output node to each power rail to prevent the output transistors from being reverse biased if an inductive load should ever cause the output node to snap to a voltage beyond the rail voltage. Reverse diodes D13 and D14 to ground from each rail prevent the rail voltage from going to a reverse polarity in the event of a fault condition, such as the failure of one rail.

Proper power supply rail decoupling is paramount in all amplifier implementations. Here the power rails are bypassed with 1000 μF right at the power transistors to minimize the amount of high-frequency current that will flow through the wiring back to the power supply. Instead, the signal current tends to circulate locally through the bypass capacitors. The ground ends of the capacitors are connected together and then their junction node is routed to the rest of the ground line to encourage local circulation of the currents and minimize the net amount of this circulating current that

passes through the main ground line. All electrolytic decoupling capacitors are bypassed with 0.1-μF metalized polypropylene film capacitors.

The power rails have been progressively decoupled from the output stage back to the pre-drivers and IPS/VAS. This further improves stability of the output Triple by suppressing inadvertent coupling at high frequencies from the output transistors back to the drivers and pre-drivers. The low R-C impedances of these decoupling networks also act like Zobel networks to damp high-frequency resonance in the rails due to wiring inductance. Finally, the added rail filtering provides a cleaner power supply to the more sensitive IPS/VAS circuits. The DC voltage drop across these R-C networks is kept below 1 V in order to preserve voltage headroom for the earlier stages.

Output Network

The main R-C Zobel network comprising C25 and R48 provides a minimum resistive load to the output stage at high frequencies, ensuring stability. Its value is relatively uncritical, but a combination of 0.022 μF and 10 Ω is used here. It should be located physically close to the output transistors, with minimal wiring inductance. At 31.6 V rms, corresponding to about 125 W into 8 Ω, power dissipation of the 10-Ω resistor will be 0.6 W at 40 kHz. A 2-W metal oxide film (MOF) resistor is used, avoiding the need for a wire-wound resistor that might be inductive. This is adequate for most normal operating conditions and full-power testing below 40 kHz. The resistor should be mounted axially ¼" off the board. A serious high-level parasitic oscillation that persists may fry the resistor, but this will be the least of one's problems.

The L-R series network consisting of L1 and R49 preserves stability with capacitive loads by isolating them from the output stage at high frequencies. Relatively small values of 2.2 Ω and 1.5 μH provide adequate isolation for this amplifier. The network becomes resistive above about 230 kHz. The impedance of the coil is about 0.2 Ω at 20 kHz. This will cause a loss of less than 0.03 dB at 20 kHz when driving an 8-Ω load. Because the impedance of the coil rises to 0.2 Ω at 20 kHz, DF at 20 kHz will be limited to about 40.

Dissipation of R49 is a concern when continuous high frequency testing is being done at high power levels. For 250 W into 4 Ω at 20 kHz, 1.6 V rms will appear across the 1.5-μH coil, resulting in 1.2 W of dissipation in the resistor. This power dissipation rises as the square of frequency. Dissipation will be about 4.8 W for continuous full-power testing at 40 kHz with a 4-Ω load. A 3-W MOF resistor is used here in recognition that high dissipation will be a rare occurrence in normal operation. This avoids the use of a wire-wound resistor. Full-power testing at higher frequencies like 40 kHz should be kept to less than 20 seconds. Full-power testing into a 2-Ω load should be limited to 30 kHz. These resistors should be mounted axially ¼" off the board. Resistor dissipation is also of concern if the amplifier breaks into a continuous oscillation at very high frequencies, but in this case overheating of the resistor might be the least of one's problems.

The 1.5-μH output coil consists of 12 turns of 18-AWG magnet wire with a diameter of 0.5". The coil length will also be about 0.5". Such a coil can be free standing, without a former. Do not wind the coil on R49. Coil doping or the equivalent should be used to hold the windings in place and damp any tendency to vibration. Self-bonding magnet wire is also available, where an adhesive layer on the surface can be activated with a heat gun. Coil resistance is about 10 mΩ, and will result in some power dissipation. Coil dissipation will be in proportion to the coil resistance as a fraction of the load impedance. If a 10-mΩ coil is loaded with 4 Ω, then the coil will dissipate 0.25% of the power in the load. If the power output is 250 W, the coil will dissipate 0.6 W. This is reasonably small and will only occur in continuous sine wave testing. The coil should be kept physically away from any ferrous materials to the extent possible, such as the enclosure if it is steel.

Speaker relay K1 provides muting, short-circuit protection and loudspeaker protection. The circuits that control it are described later. When K1 is open its NC contact shunts the loudspeaker to ground. A second 0.022-μF/10-Ω Zobel network is connected across the loudspeaker terminals. It further damps the loudspeaker side at high frequencies and helps to absorb EMI energy right at the chassis output terminals. It also provides some snubbing of the speaker relay contacts when the relay opens, reducing the degree of arcing if current is flowing when the contacts open. Rail clamp diodes D15 and D16 prevent any inductive flyback from the loudspeaker from exceeding the rail voltage when the relay contacts open. The Song Chuan 507HN-1CH-S-24VDC is a good choice for the relay. It is rated at 17 A, and has a 24-V coil.

Output stage layout

The high collector currents in a Class AB output stage are very non-linear, with a half-wave-rectified shape when the signal is a sinusoid. These currents can create non-linear magnetic fields that may cause significant distortion if they are coupled into other parts of the amplifier signal path, especially the feedback path. The sum of the collector currents of an NPN-PNP output pair must be nearly a linear representation of the signal, since this sum is nearly equal to the actual amplifier output current. This means that it is desirable to have these currents sum together with as little intervening wiring as possible, and for the loop formed by this wiring to be as small as possible.

It is also important to have a minimum of these non-linear currents flowing in the power rails or the ground. Ideally, both transistors in an output pair should be next to each other on the heat sink. Their collectors should be strongly AC coupled together with tight wiring. In designs with multiple output pairs, having all of the NPN output transistors grouped together on one side, and having the PNP transistors grouped together on the other side, is less optimal. In such a case, the path lengths to merge the resulting positive and negative rail currents are longer. Always keep in mind that current will follow the path of least impedance.

4. Heat Sink and Thermal Management

The heat sink must be sized to prevent the power transistors from becoming too hot under anticipated worst-case operating conditions. A useful criteria for selecting the

heat sink thermal resistance rating is that the heat sink not get hotter than 60 °C when the amplifier is delivering 1/3 rated power into an 8-Ω load. This is fairly conservative, and in compliance with the original FTC requirement [5]. It is less conservative when driving a 4-Ω load. A 60 °C heat sink is not dangerous to touch; you can keep touching it for about 5 seconds. Limiting the heat sink temperature to 60 °C also keeps the junctions of the output transistors reasonably cool, preserving their safe operating area. In this design a TO-220 IC temperature sensor mounted on the heat sink opens the speaker relay if the heat sink temperature reaches 70 °C. A mains thermal cutout switch can be used instead, if desired.

A typical class AB output stage dissipates about 46% of its rated power when operating at 1/3 continuous power. A 150-W version of the amplifier will thus dissipate about 70 W when driving 50 W into an 8-Ω load. With an ambient temperature of 25 °C, the temperature rise for the heat sink must be less than 35 °C, so the thermal resistance of the heat sink should be about 0.5 °C/W. With this size heat sink, the amplifier should not be operated at high continuous average power for extended periods of time into 4-Ω or 2-Ω loads.

Optional Driver Circuit Heat Spreader

For alternative physical designs where the drivers are not mounted on the main heat sink, the pre-driver and driver transistors can be mounted together on a common heat spreader. The heat spreader can be implemented with a 1" X 3" X 1/8" piece of aluminum oriented vertically. A copper strip can also be used. With pre-drivers operating at 12 mA and drivers operating at 30 mA, total power dissipation is about 5 W if rail voltages are ±58 V under no-signal conditions. Here the V_{be} multiplier transistor for the pre-drivers and drivers would be mounted on the heat spreader, and would provide about 4 V_{be} of bias voltage.

5. Protection Circuits

Current limiting and short circuit protection act to prevent destruction of the output transistors in the event of fault conditions. Loudspeaker protection safeguards the expensive loudspeakers in the event of an amplifier fault condition, such as one where a large DC voltage would appear at the output. Turn-on/off muting prevents thumps from getting through to the loudspeakers when the amplifier is power cycled. An over-temperature sensor opens the speaker relay in the event that the heat sink becomes too hot.

The protection circuits are implemented on a third board that can be mounted on top of the output board. The speaker relay and its series resistor are mounted on the output board. A suitcase jumper can connect the series resistor to ground, so that the relay can be closed for testing in the absence of the protection board. Relatively few connections are required to feed information to the protection board. The schematics of the protection circuit board are shown in Figures 3, 4 and 5.

Features of the protection circuit include:

- Current limiting of 22 A, allowing brief 480-W bursts into 2 Ω

- Speaker relay
- Short-circuit protection
- DC offset protection
- Rail voltage monitoring
- On/off muting
- Over-temperature detection

Current Limiting and Short-circuit Protection

The difference between current limiting and short circuit protection is that the former limits output current, while the latter opens the speaker relay in the event of a short circuit (and here keeps it open for 3 seconds). The *natural current limiting* implemented at the pre-driver bases by D7-10 in Figure 1 is instantaneous, and results in current clipping, while the short circuit protection circuit incorporates a delay time constant so that it is not activated for brief current spikes that are part of program material.

It is important that the short circuit protection circuit long-term (e.g., 1 second) trigger threshold be set to a lower value of current than that of the current limiting circuit. Otherwise the short circuit protection circuit will never trigger and currents at the level of the current limiting value will be allowed to persist indefinitely.

Output Transistor Safe Area

The MJL3281/MJL1302 output transistors have a safe operating area (SOA) rating of 3 A at 55 V for 1 second. For this amplifier, two pair will safely source 6 A for 1 second into a short circuit. Of course, it is likely that the power supply will sag to less than 55 V in much less than 1 second when 6 A is being sourced into a short circuit unless the power supply is extremely stiff. Note that 6 A at 55 V corresponds to 330 W peak into a 9-Ω load. For short intervals, like 50 ms, the devices can withstand significantly more current and/or voltage. They can withstand 6 A at 55 V and 3.5 A at 80 V, for example.

In the early stages of a short circuit event, the transistors will conduct much more current, as limited by the current limiting circuit. This will trip the short circuit protection and open the speaker relay within less than 50 ms. The 50-ms SOA is thus the most important parameter for short circuit protection in this design.

Current Limiting

As described earlier, flying catch diodes have been added between each end of the bias spreader and the output node to implement *natural current limiting* [1]. If sufficient current flows through the top output emitter resistors, the VAS output node will rise high enough to turn on the clamping diodes (D9, D10) at the bottom end of the bias spreader, shunting VAS current to the output node and limiting peak output current. The opposite happens if sufficient current flows through the bottom emitter resistors. In this design, these diodes limit the peak current to 11 A per output transistor, so the amplifier can produce 22 A peak.

The limit of 11 A per output device is almost 4 times the 1-second SOA of 3 A at 55 V. This current limiting alone will not provide protection against a short circuit fault, unless other means are used to keep the duration of this fault to way less than 1 second. That is the role of the output short circuit protection arrangement, wherein the speaker relay is opened in a fraction of a second.

A peak current of 22 A into a 2-Ω load will result in output voltage of 44 V, corresponding to 968 W peak, or 484 W average. This places a reasonable limit on maximum output power into 2 Ω that is about 1.6 times the maximum (voltage-limited) output for a 4-Ω load. These numbers apply only to brief bursts that do not cause significant rail sag.

Loudspeaker Relay

The amplifier employs a speaker relay that opens during muting, short-circuit, DC offset faults and over-temperature conditions. The 17-A speaker relay K1 is mounted on the output circuit board and controlled from the protection circuit board. The loudspeaker is connected to the swinger of the relay. When the relay is open, the swinger will be connected to ground, shunting the loudspeaker to ground and absorbing any EMF energy from the loudspeaker. This also prevents a contact arc from delivering current into the loudspeaker, directing it instead to ground. The second Zobel network (C26, R50) acts as a damper for the relay contacts, reducing the possibility of arcing when the relay opens. It also damps the loudspeaker during the brief interval when the swinger is open while transitioning from the NO contact to the NC contact.

A 24-V relay is used. Most relays of this type require about 0.5 W for the coil, corresponding to about 24 mA and a coil resistance of about 1000 Ω. The relay used here has a 1440-Ω coil that requires 17 mA. The relay driver circuit pulls the relay coil down to about +8 V when the relay is energized. The series resistor is thus required to supply 24 mA (with an average relay) with about 20 V across it when the rails are at 52 V under nominal 8-Ω full-load conditions. This corresponds to about 830 Ω. A 680-Ω resistor is used to provide adequate relay current under slightly worse conditions when the power supply sags at high power into a 4-Ω load.

If the rail voltages rise to 60 V under no-signal conditions, about 31 mA will flow with a 1000-Ω coil, and dissipation in R51 will be about 650 mW, allowing the use of a 2 W resistor for good margin. If a less-sensitive relay is used (e.g., lower coil resistance), a smaller value of series resistance may have to be used. A 100-μF electrolytic capacitor C26 is placed across the series resistor to create a brief high turn-on voltage to strongly activate the contact closure to aid cleaning of the contacts. K1 is closed by Q5, Q6 and Zener diode D6 when the voltage across muting delay capacitor C5 is charged to about 8.2 V.

If the signal path passes through the soft iron material of the relay frame, distortion can result. Many high-current relays are constructed this way. Try to avoid this type of relay. A suitable relay is the Song Chuan 507HN-1CH-F-S-24VDC. It features

17-A SPDT contacts and a 1440-Ω coil that requires 17 mA. It is available from Mouser Electronics.

Short-circuit Protection

The protection and speaker relay control circuits are shown in Figures 3, 4 and 5. They are implemented on a separate protection circuit board. The short circuit detection circuit is shown in Figure 3, with a single output transistor pair depicted. Output current is sensed as corresponding to the voltage drop across the 0.22-Ω R_E resistors. In a class AB amplifier with a single-pair output stage, the output current will all flow through one of the resistors, while the drop across the other is essentially zero. This observation applies to situations where the output current is substantially greater than the bias current.

The protection circuit monitors the emitter-to-emitter voltage, $V_{E\text{-}E}$, so that a positive value of this voltage indicates output current flowing in either direction (i.e., its absolute value). Indeed, with a sine wave current, $V_{E\text{-}E}$ has the appearance of a full-wave-rectified signal. For a square wave output current, $V_{E\text{-}E}$ would look like a constant DC voltage with the exception of narrow dips when polarity changes. Here the short circuit protection is triggered when the average value of $V_{E\text{-}E}$ rises to about one V_{be} after a given amount of time.

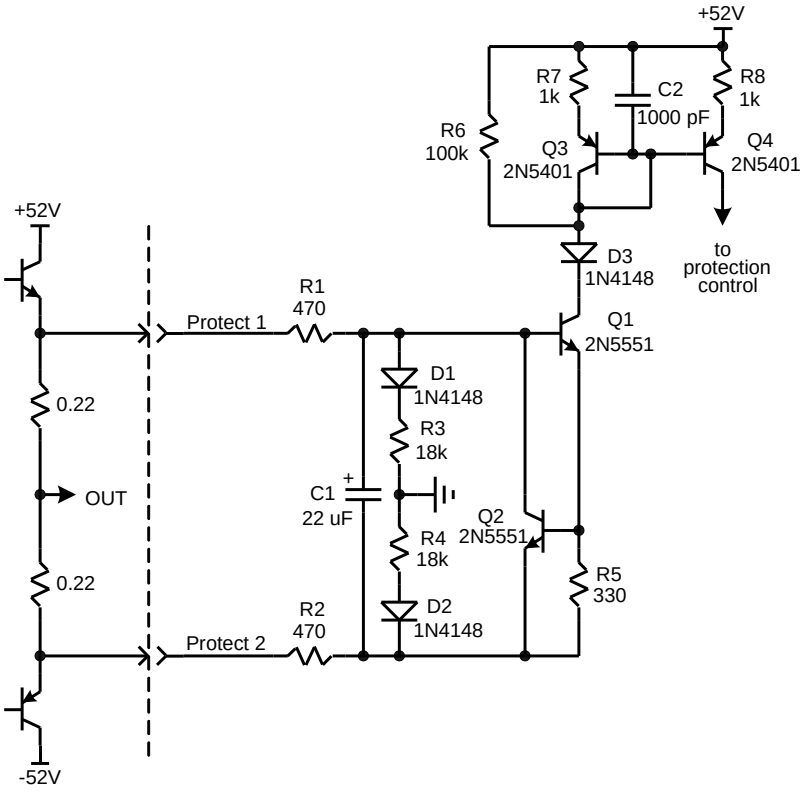

Figure 3: Short circuit detection

Q1 straddles the emitter nodes and will begin to conduct current when a filtered version of V_{E-E} reaches one V_{be}, which is about 0.55 V at 100 μA and 25 °C for the 2N5551. This voltage across 0.22 Ω corresponds to 2.5 A. R1 and R2 (470 Ω) limit base current and, in combination with C1 (22 μF), provide delay with a time constant of about 22 ms. The collector current of Q1 is mirrored by Q3 and Q4 to the input of LM339 comparator IC2-A (Figure 4) with a load resistance of 6.8 kΩ. When Q1 conducts more than 100 μA, the comparator quickly discharges C5 and opens the speaker relay. Q2 limits the current in Q1 to about 2 mA.

The long-term short circuit trigger level, I_{sc}, is about 2.7 A (100 μA, through R2 and R5, drops an additional 80 mV). The 22 ms delay time constant will allow an over-current of 4 A to persist for about 22 ms. The 50-ms SOA of the MJL3281/1302 transistors is 6 A at 55 V and 3.5 A at 80 V. An amplifier with rails that rise to 80 V under no-signal conditions may need to have a lower 50-ms trigger threshold current. One way to accomplish this is to use a transistor for Q2 that has a smaller V_{be} at 100 μA.

Also note that V_{be} conveniently decreases with temperature. One could choose a TO-126 device for Q1 and mount it on the heat sink so that its ambient temperature is closer to 40 °C, decreasing nominal V_{be} by about 33 mV. In this case, the over-current threshold will decrease further when the heat sink is hot and the SOA of the power transistors has decreased. Other circuit revisions can also be used to decrease the trigger threshold for a given V_{be}.

A larger over-current of 11 A will open the relay after only about 12 ms. These times do not include the inherent release time of the relay, which is specified as a maximum of 10 ms for the recommended Song Chuan relay. The current limiting circuit prevents the current of one output transistor from exceeding 11 A at any time. Bipolar power transistors can tolerate relatively high current for very short periods of time, even when V_{ce} is equal to the rail voltage. The output current capability is doubled for the complete amplifier here, as it employs 2 output pair (current in only one pair is monitored).

It is often desirable that I_{sc} be a function of the output voltage. There will be little or no voltage at the output under a short circuit condition. This can play a key role in distinguishing a short circuit from a legitimate high-power, high-current situation of significant duration. A high-power square wave during testing could also masquerade as a short circuit if I_{sc} is not increased for high output voltage swings. R3 and R4, in combination with D1 and D2, act to increase I_{sc} by pulling some current through R1 or R2 when the output swing is large. Note that R3 and R4 conduct no current at all until the output is at least one diode drop away from zero. In Figure 3, this arrangement increases I_{sc} to over 7 A for a peak output swing of 34 V.

Protection Control Circuit and Turn-on Muting

The protection control circuit is shown in Figure 4. It includes four sections of an LM339 comparator (IC2) to merge all of the protection functions for control of the speaker relay. If any of the open-collector outputs of sections A, B or C are low, C5 will

be discharged and the Darlington relay driver will release the relay. When all 3 outputs are high, C5 will charge through R18. When its voltage reaches about 8.2 V, after about 3 seconds, the relay driver will turn on and close the speaker relay. This provides the muting delay at turn-on to prevent audible thumps.

Each of the A, B and C sections of IC2 has a threshold of 0.7 V established by R11 and R12. Section A implements short-circuit protection. Section B implements DC offset and power–good protection based on a signal from Figure 5.

Over-temperature Protection

Section C implements over-temperature protection. If the heat sink temperature reaches 70 °C, the loudspeaker relay will open. A TO-220 LM35DT Centigrade temperature sensor, IC1, is mounted to the heat sink. It produces an output voltage of +10 mV/°C across its 10-kΩ load resistor. If this voltage reaches 700 mV, comparator IC2-C discharges C5 and opens the speaker relay. Hysteresis is provided by IC2-D to prevent cycling. The relay will not be closed again until the heat sink temperature has fallen below 60 °C. Section D is used to drive a Red LED when over-temperature is sensed.

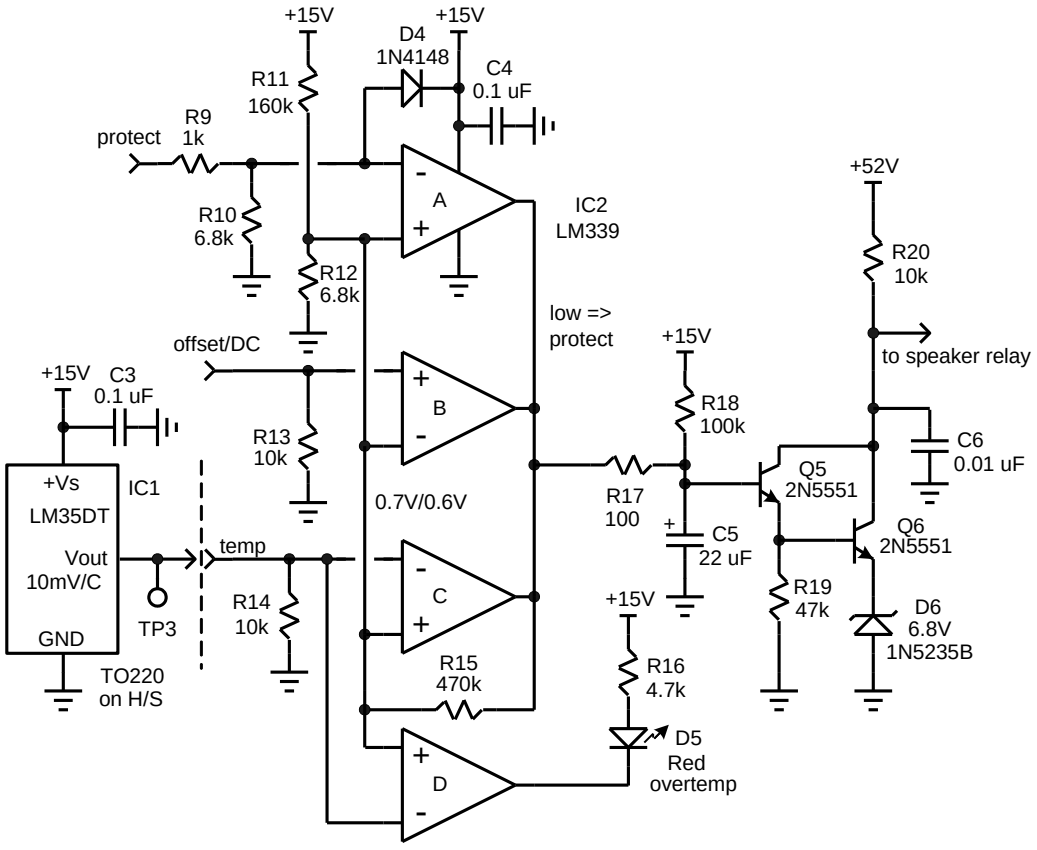

Figure 4: Protection control circuit

DC Offset Protection

A large DC offset can appear at the output of the amplifier under certain fault conditions, such as when an output transistor has failed with a collector-emitter short. This can destroy an expensive loudspeaker. DC offset protection is implemented with 2 sections of the LM339 comparator (IC3-A and B) configured as a window comparator, as shown in Figure 5.

The comparator is fed from to the output of the amplifier through series resistor R23 and delaying capacitor C7, with a time constant of 1 second. If DC offset larger than 700 mV persists for more than the time permitted by the delay, the loudspeaker relay will be opened. A DC offset of about 1.1 V in either direction will trigger protection in 1 second. The values of R23 and C7 are chosen to be large enough to prevent a 10-Hz sine wave at full power from triggering offset protection. With the values shown, if the output is stuck at a 55-V rail, the DC offset protection will be triggered in about 13 ms.

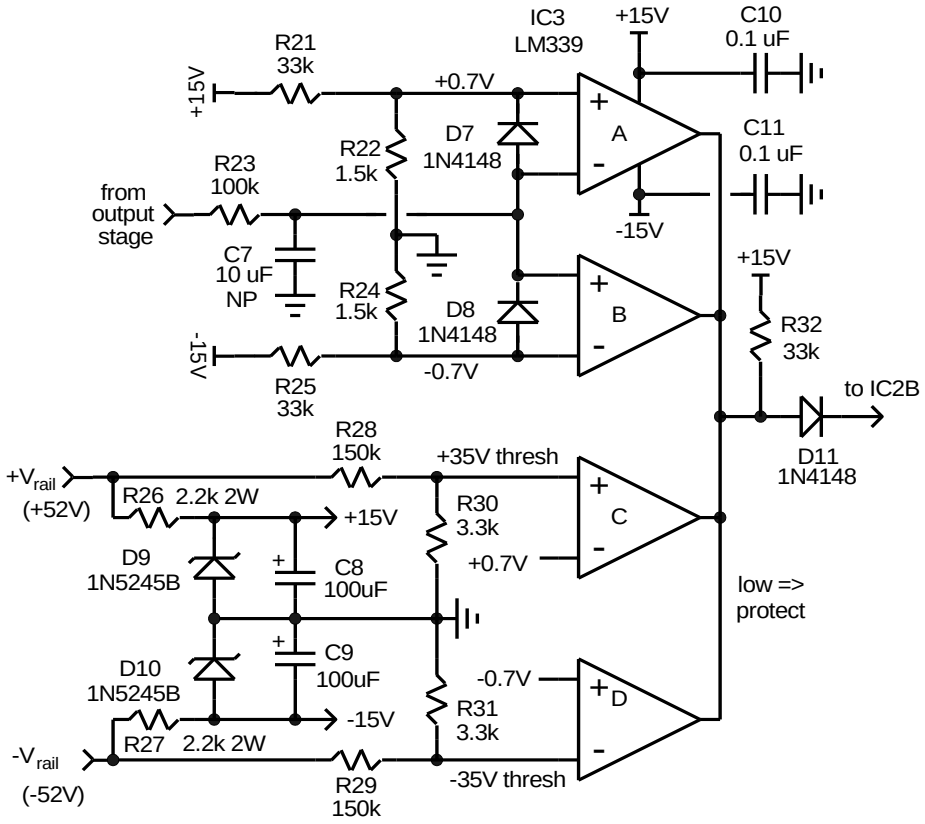

Figure 5: DC offset and power-good detect

Rails OK Protection and Turn-off Muting

This protection circuit prevents the speaker relay from closing unless and until the rails are above ±35 V. This will come into play at turn-on. More importantly, if a rail fuse blows on one polarity of rail, the speaker will be immediately disconnected. This circuit

also opens the speaker relay at turn-off before the amplifier becomes dysfunctional and might cause a turn-off thump. This circuit employs sections C and D of comparator IC3.

Powering the Protection Circuits

The protection circuits are powered by a ±15 V supply implemented with Zener diode shunt regulators D9 and D10. The 2.2-kΩ, 2-W series resistors provide 17 mA to the ±15-V rails.

Fuses

The speaker relay obviates the need for a speaker fuse. Power supply rail fusing can be used as an optional last line of defense in the event of a fault condition. If only one rail fuse blows, the rail-reversal protection diodes prevent the amplifier circuitry from being subjected to potentially damaging reverse voltages. In this amplifier, rail fusing is not used. Instead, the mains fuse is relied upon in the event of a serious over-current fault that is not handled by the protection circuits.

6. Power Supply

The power supply is very simple, incorporating a 250-VA toroidal transformer with an 84-V center-tapped secondary and a single bridge rectifier. It is shown in Figure 6. The mains side includes an IEC power connector, an X capacitor across the line, a DPST power switch and a 5-A fuse. IEC power connectors that incorporate EMI filters and sometimes a fuse and/or power switch are also available and convenient. No inrush control is employed in this design. As shown, the supply is designed to provide ±52 V rails under load at 125 W into an 8-Ω load.

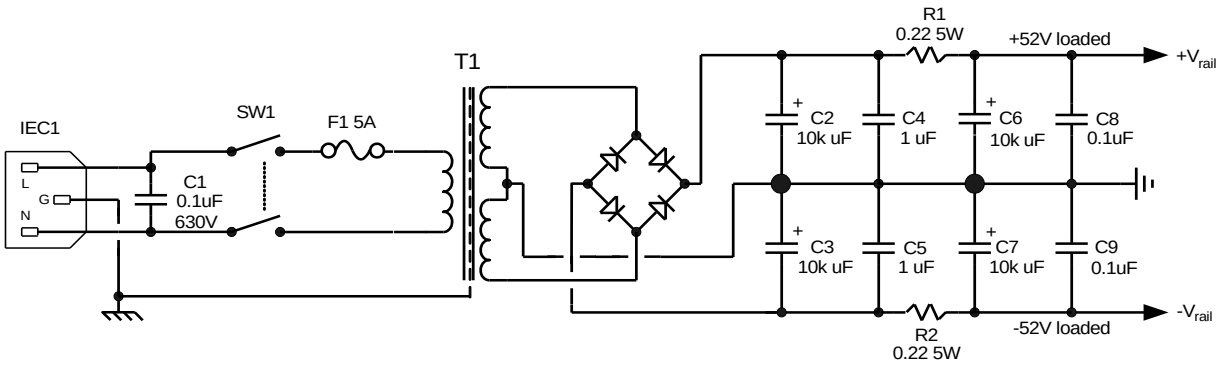

Figure 6: Power supply

The transformer can be of toroidal or conventional construction. The secondary voltage is uncritical, but will affect achievable power output. For an amplifier with only 2 output pair, the power supply rail voltages should not be greater than about ±55 V at full power into an 8-Ω load. This corresponds to an amplifier with an 8-Ω power rating of about 150 W (clipping at about 163 W). Reservoir capacitors should have a voltage rating at least 10 V greater than the anticipated no-load rail voltage.

This amplifier draws about 2 A from each rail when delivering its rated 125 W into 8 Ω. A typical power supply with an effective output resistance of 2 Ω/rail will have its rail voltages increase by about 4 V to about ±56 V under no-signal conditions. The transformer should have a rating of at least 500 VA for a 2-channel, 125-W per channel amplifier.

The bridge rectifier is a conventional 25-A, 400-V device. While not shown in the figure, snubber networks placed across each diode in the bridge are recommended. These networks can comprise 0.1-μF, 400-V capacitors in series with an optional 1-Ω resistor. Alternatively, four 25-A ultra-fast soft recovery diodes in TO-220 or TO-247 packages can be used at additional expense. The TO-247 Vishay HFA25PB60PBF HEXFRED® is a good choice. The TO-220 Kyocera FCU20A40 fast recovery diode is also a good choice. Snubbers are not required if these rectifiers are employed.

Two pair of 10,000-μF reservoir capacitors connected in a π filtering arrangement provide a total of 20,000 μF for each rail. Each 0.22-Ω series resistor creates a low-pass filter that is down 3 dB at 72 Hz and down 9 dB at the 120-Hz ripple frequency (with respect to the ripple voltage at the first reservoir capacitor). Attenuation is much greater at the higher rectification harmonics. The total amount of reservoir capacitance is uncritical, but more is usually better. Very large reservoir capacitors may dictate the use of an inrush control arrangement to avoid blowing the mains fuse.

Bleeder resistors are not used. Output stage bias current will pull the rails down until the output stage can no longer conduct bias current. This will be below about ±20 V. Two output pair will draw a total of about 240 mA, so the fall rate will be about 12 V/sec. Figure 7 shows output and ripple voltages as a function of average rail-to-rail load current for the power supply used in this amplifier.

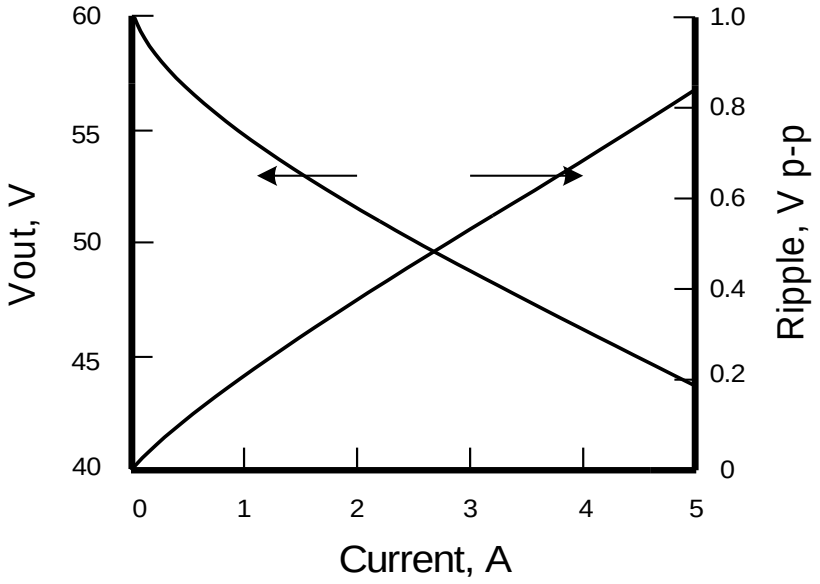

Figure 7: Power supply voltage and ripple

7. Grounding

Recommended grounding for this amplifier is quite simple. It is illustrated in Figure 8. A single ground line runs from the output end to the input end, down the center of the amplifier circuit board. The positive power rail runs along the "top" of the circuit board from left to right (as seen from the wiring side of the board), with the input end on the left. The negative rail runs along the "bottom" of the board. The rails include decoupling networks as they make their way from the output stage back to the driver stage and then pre-driver and input stages. The ground ends of each pair of decoupling capacitors are connected directly together at the center of the board, and then that node is connected by a single wire or trace to the ground bus that runs down the center of the board. Electrolytic decoupling capacitors are locally bypassed by 0.1-μF film or ceramic capacitors.

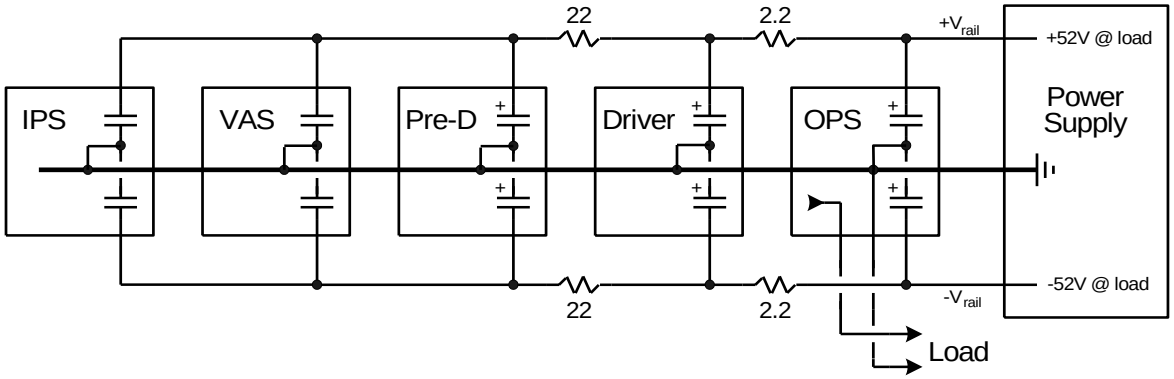

Figure 8: Grounding architecture

The positive and negative rails, and ground, are connected from the power supply to the amplifier with 3 wires twisted together. Star-quad microphone cable can be used for this short distance. Perhaps non-intuitively, the smaller AWG wire over this small distance is actually a good thing, as a small amount of resistance adds to the filtering effect of the capacitance on the output board and also encourages circulating class-AB currents to resolve locally at the output board (current takes the path of least impedance). The loudspeaker output and return terminals are both connected directly to the output circuit board, with the return connected directly to the power ground at the circuit board. Output signal currents are resolved at the circuit board.

This arrangement is not a traditional "star ground" wherein the speaker and other major grounds are returned separately to a single point ground at the power supply. In essence, the star ground is located on the amplifier circuit board. This is sometimes called a star-on-star approach.

Within the amplifier circuit board, the grounding arrangement can be described as a "tree" ground as illustrated in Figure 8. The grounding progresses from the output end

of the board back to the input end. Most of the branches are vertical conductors to the power supply decoupling capacitors located along the “top” and “bottom” of the circuit board.

8. Building the Amplifier

Simulate the amplifier first. Read about using SPICE if necessary [1]. Start by simulating some of the circuits elsewhere on this web site. The beauty of simulation is that you get to know how the circuit behaves before you build it, and what to expect when you build it. You will know what voltages to expect at every node in the circuit.

Prototyping

I always build the prototype of one channel on perf board instead of just going straight to a printed wiring board. Of course, as many do, one can go right to a printed wiring board and hope that major changes are not going to be necessary. I also find that a neat printed-wiring-board-like perf board layout can lead to a quicker, better PWB layout down the line. I am usually able to put about 90% of the interconnect on the wiring side of the board without crossovers, implementing most of the interconnect with through-hole component leads soldered to each other. Very few crossovers are needed on the component side of the board. Only a few point-to-point insulated wires are used on the wiring side. Such a layout is easily converted to a 2-sided PCB layout when the time comes. Wiring on the component side of such a layout will be fairly sparse as a result of the layout approach taken for the prototype.

9. Testing the Amplifier

The testing procedure below is very methodical and is done in recognition that the amplifier comprises three boards and the power supply. These will first be tested separately. Depending on the physical design of other versions of the amplifier, this sort of testing may not be possible.

Initial Inspection and Passive Tests

Once the amplifier is built, it is very important to test it with patience and diligence in an orderly fashion. Don’t just turn the whole thing on and hope there will be no magic smoke. Inspect and poke around a lot before powering up a prototype. Take your time and inspect every component and its connection and associated wiring for things like polarity, shorts, open joints, values, etc. Do this with an illuminated magnifier. Are any components missing? Are any transistors or diodes or polarized electrolytic capacitors installed in the wrong orientation?

Inspect and verify every path connection on the breadboard or PWB to make sure that it physically corresponds to the schematic. This is painstaking and boring, but it is well worth it for a first-time build. I cannot tell you how many times this has saved me. Not all missing or shorted connections will have fatal consequences, but finding them now will save you hours of troubleshooting later.

It is also wise to poke around with an ohmmeter to see that it registers about what you expect it to. This will often reveal shorts and opens, and sometimes wrong resistor

values. This, of course, is in-circuit testing, so some knowledge of the circuit is necessary for you to know what to expect when you probe any two points. If you don't get what you expect, find out why. It may be reflective of a circuit fault or it may be that a junction has been forward-biased by the ohmmeter current. In any case, satisfy yourself that you are getting what you should, even if it requires some further study of how the circuit should work. Sometimes an old-fashioned battery-operated ohmmeter works better for this than a DVM; see how the meter you are using reacts to reading a diode by itself in both directions.

Preparation for Testing

Initial testing of the prototype amplifier is done in several stages in a methodical approach. The power supply is tested first, by itself. The front-end board, comprising the IPS, VAS, bias spreader and pre-drivers, is tested next, in isolation. The feedback loop is closed by a jumper, which connects the center-tap of the pre-driver emitter resistors to the feedback resistor. For this test, the board is powered directly from the amplifier power supply. Some rudimentary tests are next performed on the output board by itself. The protection board is then tested. Finally, the three modules and power supply are connected together for testing of the complete amplifier.

Power Supply Test

Unlike some, I do not usually power up the amplifier with a Variac. Test the power supply by itself. This is a simple step, but worth the small amount of time it takes. Connect temporary 1-kΩ, 5-W bleeder resistors to the output rails. Apply power and make sure that all voltage readings are as expected. The rail voltages should come up quickly at turn-on. Remove the power. The rail voltages should fall slowly at turn off. A total of 20,000 μF on each rail and the 1-kΩ, 5-W bleeder resistors should result in a time constant of about 20 seconds, meaning that the rail voltage should fall to about 1/3 of its energized value within about 20 seconds after turn-off. Allow the rail voltages to fall below 3 V. This may take 2 minutes or more. The bleeder resistors are somewhat optional, but do add to safety in testing.

Front-end Test

Initial testing of the IPS/VAS and pre-drivers should be done without the output stage module. This reduces the chances that the output transistors (and possibly others) will be destroyed in the event of a serious problem in the IPS/VAS/pre-driver circuits. This testing is done with the feedback loop closed by connecting feedback resistor R8 to TP1, the junction of the pre-driver emitter resistors (R29, R30), instead of to the output rail. Short the input to ground. Connect a temporary substitute 2SC3503 V_{be} multiplier transistor to the terminals for Q14, which normally resides on the main heat sink. Adjust the bias pot full counter-clockwise to the point corresponding to lowest bias current setting.

Apply power and check the voltage at the junction of the pre-driver emitter resistors, looking for nearly zero volts within less than ±50 mV. Probe the emitters of Q15 and Q16. They should be roughly plus and minus 0.9 V, respectively. If the amplifier passes this test, this is a very good indication that the circuit is operating

properly. Probe this point with a scope to see if there is any evidence of an oscillation. Use a 10:1 scope probe or a 1:1 probe with a 100-Ω resistor in series at the tip to prevent introducing instability from probe capacitance.

Now probe numerous nodes in the front end to see that the voltages are as expected, based on voltages that were observed in simulation. Look especially at the voltage drop across resistors that are connected to the voltage rails, especially the emitter resistors of current sources and VAS transistors to verify that the proper currents are flowing. Probe the voltage at every emitter and every collector. Probe the voltages at the two bases of the input stage; they should be between +50 and +300 mV, and within ±20 mV of each other. I always make such measurements with a 1-kΩ resistor in series at the end of the DVM probe to make sure that probe capacitance does not inadvertently cause an oscillation when touching a sensitive node.

Check the voltages at the top and bottom of the bias spreader. The magnitudes of these bias voltages should be about the same, at about ±1.5 V with respect to ground with the pot set for minimum bias. Adjust the 10-turn bias pot clockwise by a couple of turns and observe increased voltages. Adjust the pot full clockwise and observe voltages on the order of ±2.4 V. Check the voltages at the emitters of the pre-driver transistors and observe that they are on the order of ±1.7 V. Reduce the bias setting to the minimum and observe that these voltages are on the order of ±0.9 V. As a final DC check, touch all of the transistors and verify that none is hot.

Initial Small-signal Front-end Test

With the front-end working properly, perform small-signal and large-signal testing of the circuit with an audio generator, scope and AC voltmeter. The audio generator and AC voltmeter should operate to at least 1 MHz. The scope should go up to at least 20 MHz. If you don't have this equipment, obtain it. Ebay can be your friend here, especially for a good used, working oscilloscope. Alternatively, shop around for new equipment. Some good PC-based oscilloscopes are available at reasonable prices. Web searches with terms like PC-based oscilloscope or other terms like audio oscillator or function generator can bring up many good choices.

Connect the scope and AC voltmeter to the output (junction of pre-driver emitter resistors). With the input grounded, there should be a clean, noiseless line on the scope with its sensitivity set to 1 V/division. There should be no evidence of any parasitic oscillation or line ripple. The AC voltmeter should read less than 10 mV rms. Remove the input short and see the same performance with the open input.

Apply 100 mV rms at 1 kHz to the amplifier input and observe a clean sine wave at the output that measures about 2.7 V rms. Sweep the frequency from 20 Hz to 20 kHz and observe a flat frequency response within +0, -0.2 dB with respect to the 1 kHz amplitude. Sweep the frequency from 20 Hz to 1 MHz and observe frequency response within +1, -10 dB with respect to the 1 kHz level. Observe that the output amplitude is down 3 dB at about 550 kHz. Lift input low-pass filter capacitor C3. HF response should be down 3 dB at about 1.1 MHz. Replace C3.

Apply a 200-mV p-p 10-kHz square wave to the front-end and observe a well-behaved 5.5 Vp-p square wave on the scope, with minimal ringing and overshoot. A multi-cycle burst of decaying ringing following the edges of the square wave is an indication that there is a problem with the feedback compensation. Ringing is usually accompanied with a peak at some frequency in the small-signal frequency response. Rise time from 10-90% should be about 0.5 μs.

Initial Large-signal Front-end Test

The amplifier IPS/VAS/pre-driver circuits should now be tested with large signals. Set the scope to 10 V or 20 V per division, using a 10:1 probe if necessary. Set the generator frequency to 1 kHz and gradually increase the level up to 1 V rms. The signal should remain clean and rise to 27.3 V rms. Increase the level gradually until the output exhibits minor clipping. The signal should remain clean, with no sign of oscillation, even before and after the clipping points. The output level at this point should be on the order of 30 to 40 V rms, depending on rail voltages. The peak voltage at clipping should be no more than 3 V below the rail voltage. Positive and negative clipping should be reasonably symmetrical. There should be little evidence of power supply ripple modulation. Increase the signal level further until harder clipping is evident and observe that the circuit is still behaving well.

Protection Circuit Test

Prepare the protection board for testing. Connect the DC offset input end of R23 to ground. Connect a 2.2-kΩ, 5-W resistor from the speaker relay output to the +52 V supply. Connect the protect 1 and protect 2 input terminals both to ground. Connect a voltmeter from the relay output to ground. Connect the board to the power supply.

Apply power. The relay voltage should drop to about +8 V after about 3 seconds. Verify that the voltages at C8 and C9 are +15 V and –15 V, respectively. Apply +1 V to the DC offset input. The relay voltage should go to the +52 V rail voltage within 1 second. Remove the voltage from the DC offset input and connect the input to ground. The relay voltage should drop down to +8 V after about 3 seconds. Apply –1 V to the DC offset input. The relay voltage should go to the rail within 1 second. Remove the voltage from the offset input and connect the input to ground. The relay voltage should drop down after about 3 seconds.

Apply +0.8 V to the temperature sensor input at R14 and IC2C. The relay voltage should go high immediately. Remove the voltage from the sensor input. The relay voltage should drop down after about 3 seconds. Apply +1 V to the protect 1 pin. The relay voltage should go high immediately. Remove the voltage from the protect 1 pin and connect the pin to ground. The relay voltage should drop down after about 3 seconds. Apply –1 V to the protect 1 pin. The relay voltage should go high immediately. Remove the voltage from the protect 1 pin and connect the pin to ground. The relay voltage should drop down after about 3 seconds. Connect a voltmeter to the +52-V rail. Turn off the power. The relay voltage should go high at about the time when the rail voltage has fallen to 35 V. This completes testing of the protection board.

Output Module Test

Here some brief testing of the output module and the protection circuit board is done. Temporarily connect the driver inputs of the output module to ground through 100-Ω resistors. Connect the power supply to the module and apply power. All transistors should remain cold and the driver emitter resistor center tap and the output rail should be at ground potential. The output bus should be at ground potential. Connect the loudspeaker relay series resistor R51 to ground and observe that the relay closes.

Remove power and connect the protection circuit board to the output module. Apply power and verify that there is a 3-second delay before the speaker relay closes. Remove power and observe that the relay opens after several seconds.

Test the complete amplifier

With a known-good, thoroughly tested IPS/VAS/pre-driver, it is now time to test the amplifier as a whole, with the output stage connected to the front-end. Having spent the time in testing as described above, it is now much less likely that destruction will occur when the output stage is included. Remove the temporary feedback connection that was made to the center of the pre-driver emitter resistors and connect R8 to the output rail. Remove the temporary 100-Ω resistors at the driver base inputs of the output module. Connect the pre-driver outputs to the output module. Set the bias pot counter-clockwise for minimum bias. Short the amplifier input.

Apply power and verify that there is a 3-second delay before the speaker relay closes. Observe 0 V ±50 mV at the amplifier output. Measure and record the rail voltages and observe that they are not significantly lower than they were in earlier tests. Verify that the voltages at the rail filter capacitors are approximately the same as those at the power supply, with voltage drops of less than 1.5 V as the measurement points move from the amplifier output stage toward the amplifier input stage. Kill the power and verify that the speaker relay opens when the power supply rails fall below about ±35 V.

Bias Adjustment

Apply power. While probing across one of the NPN output transistor emitter resistors (e.g., R44) with the DC voltmeter, gradually turn the bias pot clockwise, increasing the bias setting, until there is 10 mV across the emitter resistor. Observe that there is no oscillation and that the output of the amplifier is within ±50 mV of ground. Place the DVM across each of the other emitter resistors and observe that there is between 1 mV and 20 mV across each of them. Ideally they should all have 10 mV across them, but V_{be} mismatches among the output transistors may introduce differences.

Increase the bias until there is on average about 26 mV across all of the emitter resistors. Record the voltage seen across each emitter resistor. Check the rail voltages and observe that they have sagged just a bit due to the fact that the output stage is now drawing over 200 mA. Observe that the power transistors will begin to get warm. Leave the amplifier on for 30 minutes and then observe that the voltages across the emitter resistors have not changed by more than 10 mV from their previous readings.

No-load Test

Connect the scope and AC voltmeter to the output rail of the amplifier (ahead of the output coil). Repeat the small-signal testing that was done on the IPS/VAS/pre-driver circuits earlier, using a 200-mV rms input signal. This should generate 5.45 V rms at the output. Similar results to the earlier small-signal tests should be seen. There should be no evidence of oscillation or high-frequency gain peaking greater than 1 dB. Repeat the large-signal testing that was done earlier on the IPS/VAS/pre-driver, observing similar results. The peak voltage at which clipping occurs may be up to 1.4 V less than seen before.

Small-signal Test Under Load

Reduce the input signal level to zero and connect an 8-Ω, 50-W dummy load to the amplifier output. It can be a heat-sink-mounted power resistor. It is not important that it be non-inductive. Repeat the tests that were conducted above for small signals, with an AC voltmeter and scope connected to the output terminal of the amplifier. Expect similar results. Amplifier gain should not be reduced by more than 0.2 dB from the no-load value. Frequency response should be down by 3 dB at about 330 kHz ±50 kHz. This includes the bandwidth-limiting contributions of the input filter and the output L-R network. Accuracy of the 1.5-μH inductor will not have a significant effect on amplifier performance, but it will have a significant effect on the frequency at which response is down 3 dB. If the output is probed ahead of the L-R network, the response should be down 3 dB at about 560 kHz ±100 kHz.

Large-signal Test Under Load

Set the signal generator to zero volts at 1 kHz. Output power levels greater than 50 W should be limited to less than 30 seconds to avoid overheating of the load resistor. Repeat the large-signal testing that was done above under no-load conditions. Clipping signal voltages will be a few volts less than observed under no-load conditions due to power supply sag and signal voltage drop across the R_E resistors. Measure the rail voltages at just under clipping at 1 kHz and record them. Compare them to the no-load values and observe the amount of power supply rail sag under full load. Although not critical, it is desirable that the amount of sag from no-load to the loaded condition should be less than about 5 V. This is a measure of the stiffness of the power supply.

The amplifier should also be tested under large-signal conditions with a 4-Ω load. Running this test at near full power is optional and requires the use of a higher-wattage load resistor. The amplifier may output up to 250 W or more in this test. A second 8-Ω, 50-W resistor can be placed in parallel with the original 8-Ω load. This will suffice as long as the duration of the test is limited to about 30 seconds.

Temperature Test

Operate the amplifier at approximately 1/3 power with an 8-Ω load at 1 kHz for 15 minutes. This corresponds to about 50 W (20 V rms), and is the approximate power level at which amplifier dissipation is maximum . Periodically touch the heat sink with your index finger. At no point should it get so hot that you cannot keep your finger on the

heat sink for at least 3 seconds. This will verify that the heat sink temperature does not rise above about 60 °C under those conditions. Probe TP3 at the output of IC1 and read the heat sink temperature as the voltage reported by the LM35 multiplied by 100 °C.

Capacitive Load Test

Amplifier stability under capacitive loading conditions is verified in this test. Apply a 200-mV p-p 20-kHz square wave to the input of the amplifier with an 8-Ω load. Sequentially apply 1000-pF, 0.01-μF, 0.1-μF and 1-μF capacitances across the load and observe on the scope that there are no parasitic oscillation bursts anywhere on the output signal. There should be no multi-cycle ringing bursts at the edges of the square wave that do not decay fully within 3 cycles. Some overshoot and minimal ringing may be seen on some of these tests. No overshoot or ringing should be seen with 1000-pF or 0.01-μF loading. With 0.1-μF loading, 6% overshoot with no ringing will be seen. With 1-μF loading, 74% overshoot with one cycle of ringing will be seen. If the output is probed before the L-R network, only 2% overshoot will be seen, confirming that virtually all of the overshoot at the output is due to the highly-damped resonance of the L-R network and the load capacitance.

Repeat these tests with a 1.2 V p-p square wave at the input to verify large-signal stability with a 33-V p-p output. Results should appear similar. With 0.1-μF loading, the amplifier is called upon to deliver 6.5 A peaks into the load. With 1-μF loading, the peak current delivered is on the order of 20 A. This latter condition approaches or exceeds the current limiting value of the amplifier.

DC Offset Protection Test

Briefly connect a 1-MΩ resistor from the positive rail to the junction of R23 and C7 on the protection board (Figure 5). The speaker relay should open in less than 1 second. It should close about 3 seconds after the 1-MΩ resistor is removed. Repeat the test with the resistor connected to the negative rail.

Short-circuit Test

This is the scary test. It is optional, and not for the faint of heart. Failing this test may result in magic smoke. Briefly connect a 47-kΩ resistor from the positive rail to the base node of Q1 on the protection board (Figure 3). The speaker relay should open. After removal of the 47-kΩ resistor, the speaker relay should close in about 3 seconds. This procedure tests most of the short circuit protection circuitry.

With the amplifier input shorted, short the output terminals. You should hear the speaker relay open quickly. Immediately remove the short circuit when you hear the relay open. About 3 seconds later you should hear the speaker relay click again as it closes. Check the output for less than ±50 mV offset. Apply 100 mV rms at 1 kHz to the input. Repeat the above test with a scope attached to the output. The 1-kHz sine wave should re-appear after the relay closes following the removal of the output short. Note that this protection circuit will “retest” for a short circuit about every 3 seconds.

Stability Evaluation

Adequate phase and gain margins can be verified by checking frequency response or square wave response with the feedback network temporarily modified. This is done with input filter capacitors C1 and C3 disconnected and with the amplifier output measured before the L-R output network so that the wideband response of the amplifier is measured. The connection at the junction of feedback resistors R7 and R8 is altered to introduce added phase lag or to decrease closed-loop gain. These tests do not measure phase and gain margin as such, but rather verify that there is enough.

Shunt R8 with a 10-kΩ resistor to increase closed-loop gain by 3 dB. Shunt the junction of R7 and R8 to ground with a 39 pf capacitor. This introduces a pole and 3 dB of loss at 1 MHz. Existing phase margin has now been reduced by 45 degrees. If the amplifier does not oscillate, it has at least 45 degrees of phase margin. Measure the amount of peaking in the frequency response. Peaking of 3 dB would suggest a phase margin of 45 degrees. Expected peaking in this test should be on the order of 8 dB at about 1 MHz. Response will be down about 3 dB at about 2 MHz.

Remove the resistor and capacitor added above. Short R8. This will decrease closed-loop gain by about 6 dB. If the amplifier does not oscillate, it will have at least 6 dB of gain margin. Under this condition, closed-loop bandwidth will be on the order of 3.6 MHz with no peaking.

Further Testing

You now have a working amplifier and you can proceed with other performance tests, such as THD.

10. Troubleshooting

If the amplifier does not work at any point in the process, troubleshooting is necessary. A great deal of the testing outlined above is also done for troubleshooting. This is particularly so for voltage measurements. If an amplifier is built for the first time and passes the initial testing in the order described above, it is very likely that it will work. Of course, if problems occur at one of those steps, troubleshooting is called for. The sequencing of the tests helps to localize where the problem is. If an already-built amplifier does not work, or has never worked, the troubleshooting described here is especially helpful.

Always start by carefully inspecting the amplifier, often with an illuminated magnifying glass. Look for parts that appear to be damaged in any way. Look for shorts or opens. Verify proper part values and part orientation.

If the amplifier is known to have experienced damage, as with burned parts or suspected blown transistors, it is especially important to make sure that any and all blown transistors are replaced before powering up the unit with the replaced components. Transistors can often be evaluated in-circuit for having been blown. The collector-base or base-emitter junction is usually shorted if the transistor is blown (unlike a fuse, which blows open). I always check with an old-fashioned battery-operated passive ohmmeter,

often on the 100-Ω range. The meter will usually apply enough current to forward-bias a junction. A shorted junction will read zero ohms. A good junction will usually give a reading about ¾ the way up the meter scale.

If the amplifier blows up when turned on, and if there are no bad transistors, be especially careful to make sure that the bias pot has been set to minimum bias and that the bias spreader is working properly. Check to see if the amplifier operates if the output stage is disconnected and with the negative feedback taken from the pre-driver emitter resistor center tap (TP1). This connection will often be tolerant of bias spreader voltage set too high, and allows verification that the bias spreader voltage has been set for low bias.

If the output of the amplifier is stuck at one rail, measure the voltages at each signal path node to see if they are nominal, stuck high of normal or stuck low of normal. Always note the correspondence between input and output voltages of a stage. For an inverting stage, the input and output voltages should be of opposite relative polarity. Find where in the complete feedback loop the voltage level or polarity is not what it is supposed to be given the state of the input voltage to that stage.

11. Performance

The performance of the amplifier is summarized here. With 52-V rails (under load) the amplifier clips at about 135 W into an 8-Ω load. Depending on power supply stiffness, the 52-V rail may rise to 60 V under a no-load condition, suggesting momentary clipping power of perhaps 190 W.

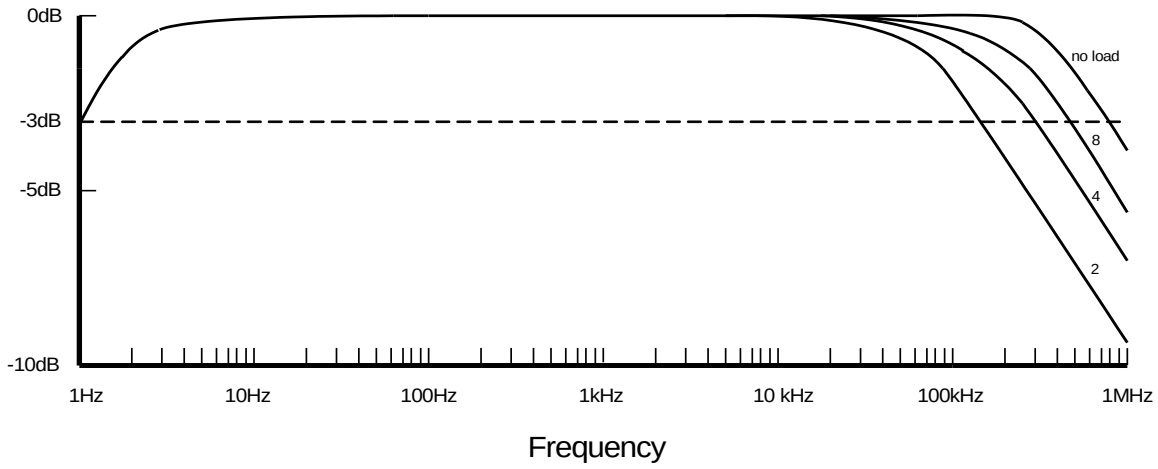

Figure 9: Frequency response

Frequency Response

Bandwidth at –3 dB extends from 1 Hz to 340 kHz with an 8-Ω load. The high-frequency 3-dB point is dominated by the input filter and output network. Without the output network, the HF response extends to about 560 kHz. Without the output network

or the input filter, the HF response extends to about 1.1 MHz at –3 dB with less than 0.5-dB peaking. Measured frequency response for no load and 8-Ω, 4-Ω and 2-Ω loads is shown in Figure 9. Square wave response at 10 kHz is shown in Figure 10 (10 V p-p, 8-Ω load). Bandwidth of the amplifier for 4-Ω and 2-Ω loads is 270 kHz and 150 kHz, respectively.

Square Wave Response

Apply a 200-mV p-p 10-kHz square wave to the amplifier and observe a well-behaved 5.5-V p-p square wave at the output. Fairly sharp edges and no ringing should be observed. Repeat the test with a 100-kHz square wave. Rise time (10% to 90%) should be about 1.2 μs.

Slew Rate

Slew rate for the amplifier is +56 V/μs and -63 V/μs when measured without the input low-pass filter and before the output L-R network. Slew rate is measured with a 2-V p-p, 100-kHz square wave.

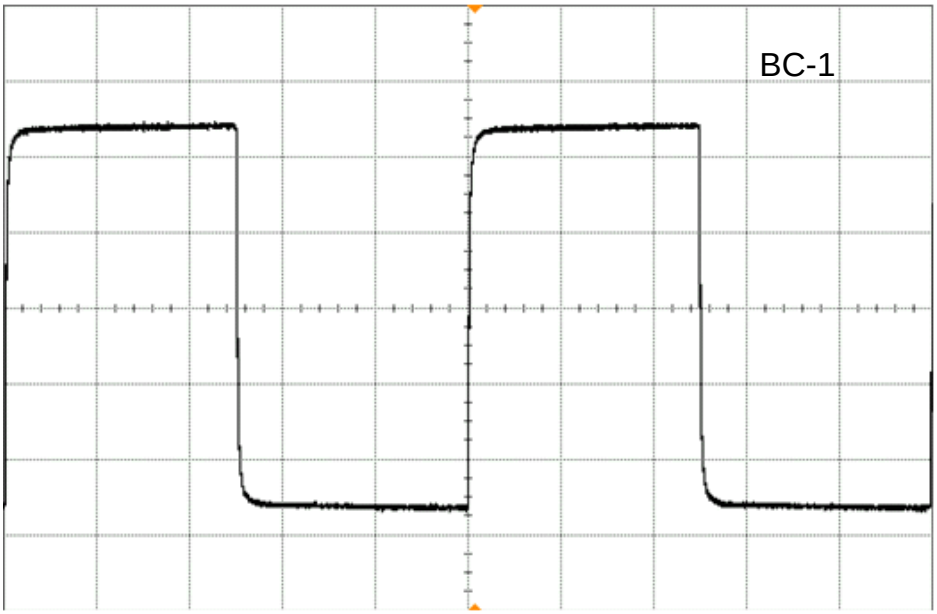

Figure 10: 10-kHz square wave response

THD+N

Measured THD+N versus power at 1 kHz and 20 kHz is shown in Figure 11 for 8-Ω and 4-Ω loads. The dotted curves show THD-1 by itself at low levels, demonstrating that the rising THD+N at low levels is noise as opposed to crossover distortion. THD+N versus frequency at 125 W is shown in Figure 12**.**

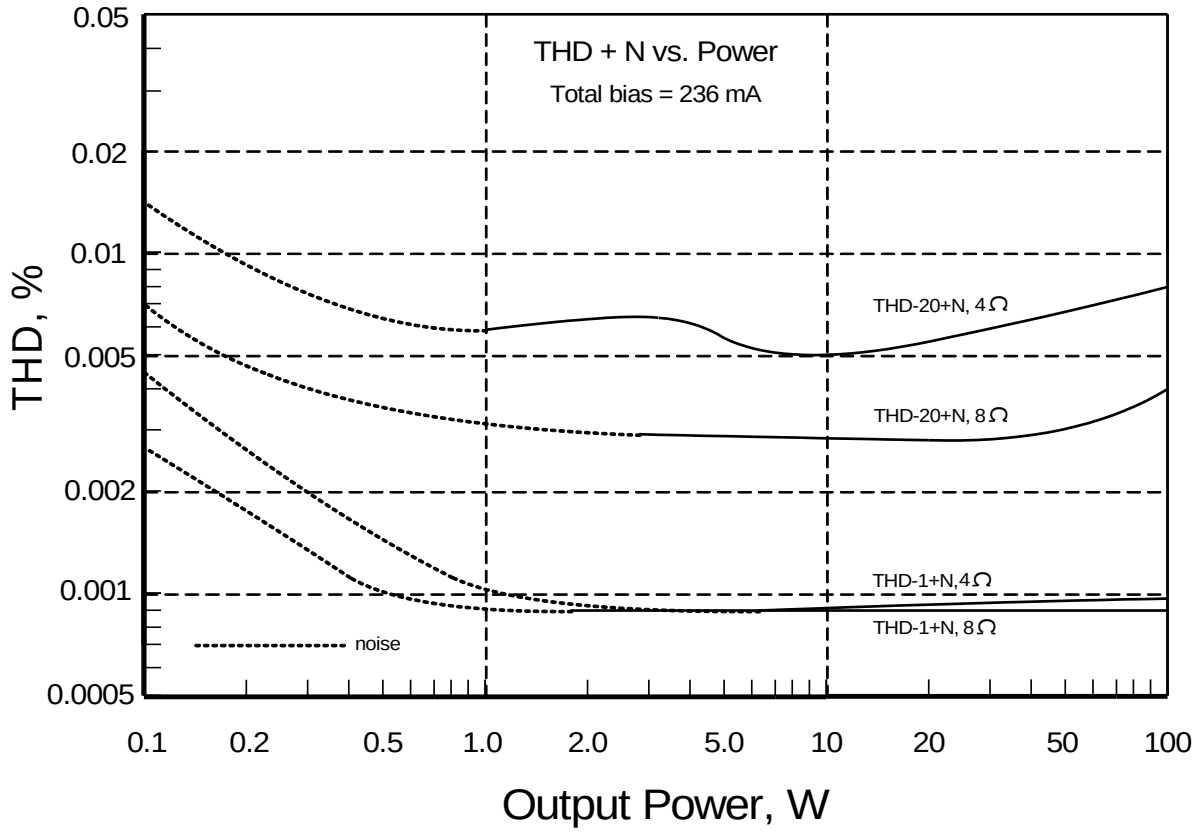

Figure 11: Measured THD+N vs. power at 1 kHz and 20 kHz

Simulated and measured THD-1 at 125 W into 8 Ω are 0.00015% and 0.0005%, respectively. Simulated and measured THD-20 at 125 W into 8 Ω are 0.0034% and 0.004%, respectively. Measurement results are in reasonable agreement with simulation results, and this is encouraging. The simulated results do not include noise, so measured THD+N is higher than simulated THD at lower power levels. THD-1 without noise was also measured by connecting a spectrum analyzer to the distortion analyzer output. It measured less than 0.001% for all power levels up to 125 W into 8 Ω. The Distortion Magnifier discussed in Chapter 26 of Ref. 1 was used to make some of these measurements [6].

The THD versus frequency plot in Figure 12 shows the decreasing reduction of THD by negative feedback as frequency rises. The distortion at 100 W is rising at about 6 dB/octave between 10 kHz and 20 kHz, the same slope as the feedback loop gain is falling, indicating that dynamic HF distortion in the output stage is quite small.

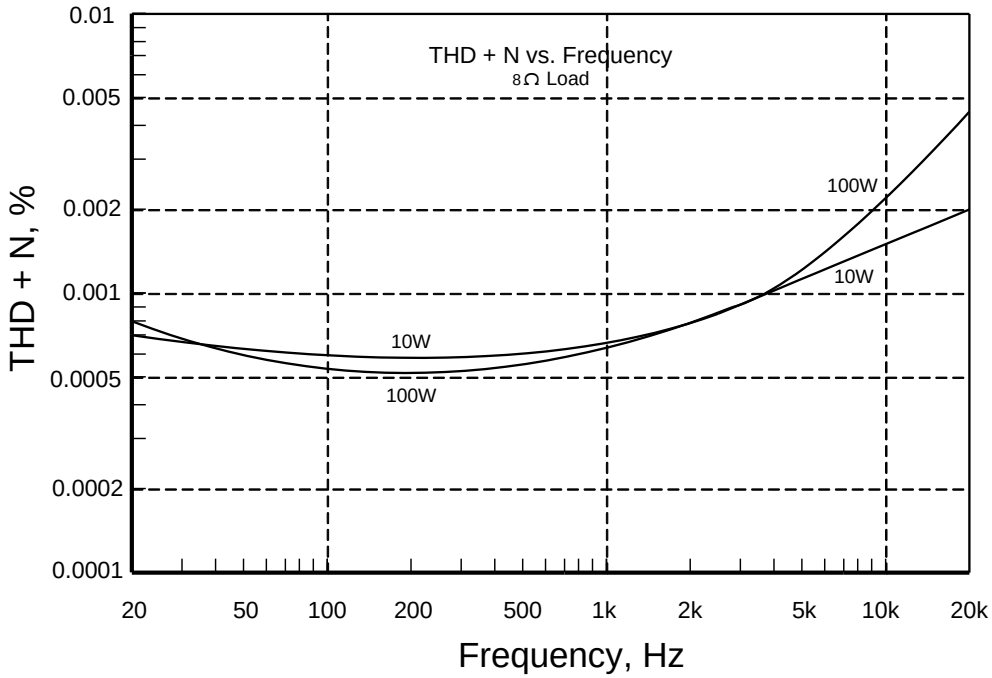

Figure 12: THD+N vs. frequency at 10 W and 100 W with 8-Ω Load

The THD vs. frequency plot in Figure 12 is quite boring, and basically shows the decreasing reduction of THD by negative feedback as frequency rises. Notice that the higher distortion at 10 W reflects the increase in THD at lower power levels due to crossover distortion in the output stage. The distortion is rising at 6 dB/octave, the same slope as the feedback loop gain is falling, indicating that dynamic HF distortion in the output stage is negligible.

Crossover Distortion

The output stage is usually the largest contributor to distortion in well-designed amplifiers. This is easily seen when one observes the increase in amplifier distortion with heavier loading. As discussed previously, the output stage bias current plays a significant role in the amount of crossover distortion created by an output stage. Biasing the output stage to the Oliver criteria of V_t = 26 mV across each emitter resistor is supposed to minimize crossover distortion in the ideal case [4]. Most amplifiers do not conform to the ideal case, however. Real-world factors like ohmic emitter and base resistance in the output transistors, and the resistance of base stopper resistors tend to reduce the value of V_t that minimizes crossover distortion. These resistances, as seen looking into the emitter, act as extensions of R_E, making the effective value of R_E larger and the optimum bias current smaller.

Figure 13 shows measured output stage THD-1 as a function of power for 4 different values of V_t. Output stage distortion was measured by operating the amplifier normally, but connecting the distortion analyzer to the pre-driver emitter resistor center

tap (TP1). This technique exposes the output stage distortion, as long as the global negative feedback forces the distortion at the output of the amplifier to be much smaller.

As expected, the optimum value of V_t is less than 26 mV and the crossover distortion rises and then decreases as power is reduced from a high value. Here the optimum value for V_t is less than 20 mV. It is also evident that crossover distortion is not overly sensitive to changes in bias current over a reasonable range, the maximum value changing by only a factor of 1.5 as V_t moves from 20 mV to 30 mV (corresponding to bias current per output pair moving from 91 mA to 136 mA. Maximum crossover distortion occurred at 5 – 7 W, and was no more than 1.8 times full-power distortion. With the best bias setting of 20 mV, the distortion maximum (0.053%) was only 1.2 times higher than that at full power (0.045%).

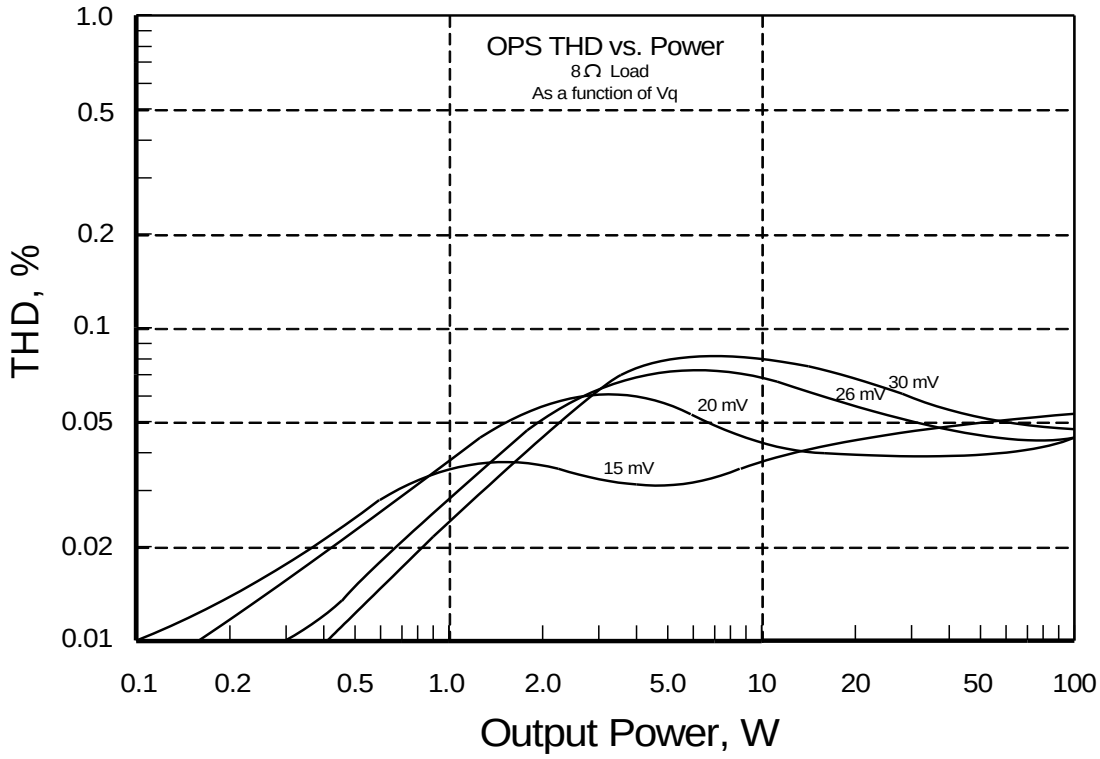

Figure 13: Output stage THD-1 vs. power for different bias current

Noise

Input-referred noise of the amplifier is 7.5 **nV/rt Hz**. This is very respectable. A-weighted S/N is an excellent 102 dB with respect to 2.83 V output (1 W into 8 Ω). Un-weighted S/N with respect to 2.83 V is 100 dB in a 20-kHz measurement bandwidth. Resistors R4 and R6, each 1 kΩ, are by far the largest noise contributors. Halving the value of these resistors would reduce their contribution by 3 dB, but would reduce amplifier input impedance to about 13 kΩ unless some other circuit approaches were used.

Damping Factor

Damping factor (DF) as a function of frequency is shown in Figure 14 below. DF is over 200 from 20 Hz to 2 kHz and falls to 47 at 20 kHz. DF is limited primarily by the impedance of the output network. Absent the output network, DF is 800 at 1 kHz and 400 at 20 kHz. Output impedance at 1 kHz is 10 mΩ. The extremely low output impedance is due primarily to the use of an output Triple in combination with high loop gain, especially at low frequencies. Loop gain is about 92 dB at 20 Hz. More specifically, closed-loop output impedance is very low because open-loop output impedance is very low and is very much reduced by the high negative feedback loop gain. Open-loop output impedance is low because the shunt feedback of the Miller compensation keeps the output impedance of the VAS low, and that impedance is greatly reduced by the very high current gain of the triple-EF output stage.

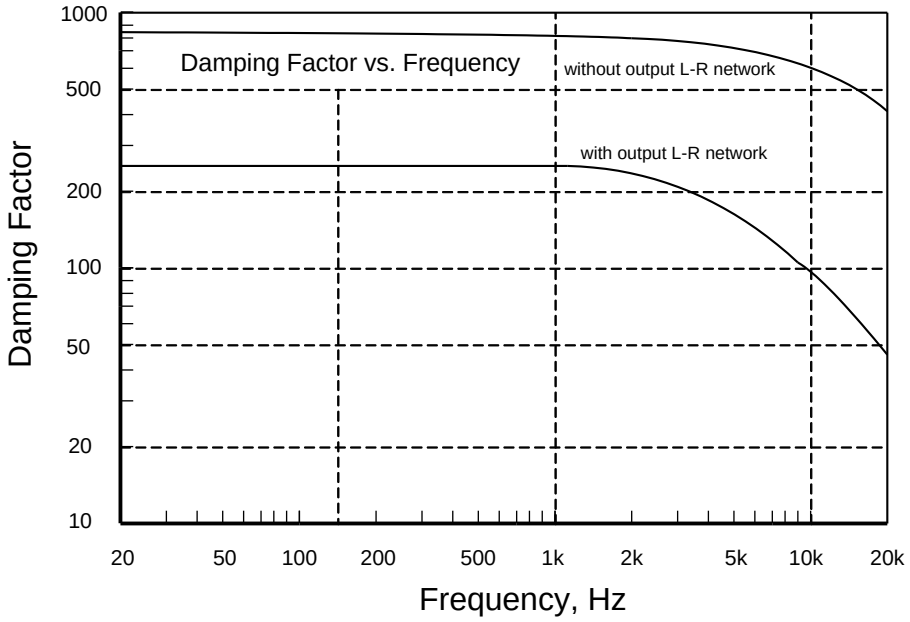

Figure 14: Damping Factor vs. frequency

12. Scaling

This amplifier is designed with transistors that can handle relatively high power supply rail voltages and the operation of the circuits is also not strongly dependent on rail voltages. As a result, the design can be scaled for different power output capabilities by selecting the appropriate power supply rail voltages and employing an adequate number of paralleled output transistor pairs. As shown, the 2-pair design is adequate up to about 150 W with an 8-Ω load.

As an example of scaling, an implementation of the BC-1 amplifier with a power supply of higher voltage was conservatively rated at 150 Watts into 8 Ω with power rails of ±64 V at idle and falling to ±58 V when delivering 150 Watts. That design is rated at

230 W into 4 Ω with the power supply sagging to ±54 V. Clipping points were 175 W and 280 W, respectively. The BC-1 is capable of more power with higher supply rails or stiffer supply rails.

The BC-1 can also be scaled in the number of output transistor pairs. Although the design here employs two pairs, higher-power versions of the design can be implemented with 3 or 4 pairs with no difficulty.

The maximum peak output current allowed by the current limiting circuit will be proportional to the number of output pairs, while the maximum V_{ce} that the output transistors will see is roughly proportional to the square root of the maximum power level for which the amplifier is designed. Bear in mind that if a stiff power supply is used, the maximum output power for a 125 W amplifier will be nearly 250 W into 4 Ω and 500 W into 2 Ω, assuming that current limiting does not occur. If the amplifier drives 40 V peak into 2 Ω, 20 A will be required, which is about the maximum for this 2-pair design. That corresponds to 400 W.

This is a sobering reminder of the need to over-design the output stage if the amplifier will ever see a load much less than 4 Ω. A single pair of output devices will suffice up to about 75 W into 8 Ω and still be adequately robust. In very rough terms, one can safely go up by 75 W/8 Ω for each pair of output devices. A 4-pair design thus will be capable of about 300 W into 8 Ω with rail voltages of ±75 V. This very rough rule-of-thumb assumes that the thermal resistance of the heat sink is low enough to keep the heat sink temperature below 60 °C.

Inrush Control

If the power supply is equipped with an NTC inrush control device, some effective resistance will be added to the supply by that device, slightly reducing maximum power. However, the inrush device can be shorted by a relay once adequate rail voltages have been reached. In this design, a relay controlled by the same circuit as the speaker relay can be added to short the NTC resistor after turn-on. More on this can be found in Ref. 1.

Quasi-boosted Supply Rails

A separate power supply rectifier and reservoir capacitors can be used for the front-end. This increases nominal available voltage under load, decreases rail drop under transient load, and can reduce ripple. It also provides more voltage headroom for the VAS for brief periods when the amplifier is delivering high current to the load. It is a relatively inexpensive upgrade, as the added rectifier and reservoir capacitors can be relatively small.

13. Printed Wiring Board Availability

Printed wiring boards for the BC-1 amplifier are available on eBay at

BC-1 Amplifier pcb set , ~150-200 W/ch/8ohms stereo (Class-AB) | eBay

The PCBs come with all of the build documentation, including a Mouser BOM that makes it easy to order the parts. Some part designations and values will be slightly different than shown here due to some revisions and improvements to the design after this document was created.

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